3D Integration for Integrated Circuits and Advanced Focal Planes

Fermilab Colloquium

February 28, 2007

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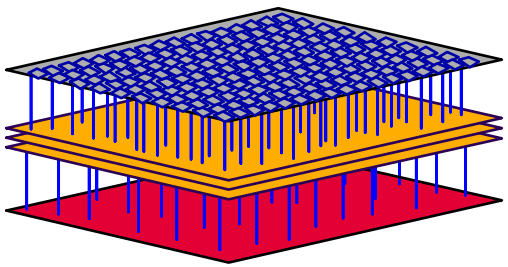
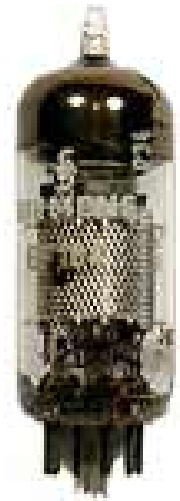


*****_This work was sponsored by the Defense Advanced Research Projects Agency under Air Force contract #FA8721-05-C0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government ._

Outline

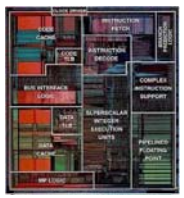
- A brief history of CMOS scaling
- Drivers behind “Moore’s Law” and their future outlook
- The potential of “Next Generation” technologies beyond silicon CMOS
- 3D circuit integration technology and applications
- Summary

A Few Metrics



- **Vacuum tube (early 1900's) – transistor (1949) – integrated circuit- IC, "chip" (1959)**
  - **During the first 10 years of the chip's development the US government bought the majority of all ICs produced**
  - **Today the US Government purchases are a few percent of the market**

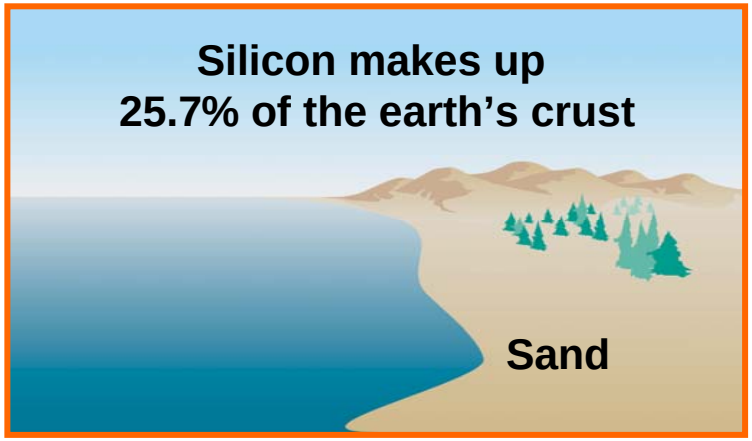
- **Today's microprocessors contain >500 million transistors and occupy ~2-3 cm^2 area**
  - **Equivalent number of vacuum tubes would cover an area equal to ~250 football fields**

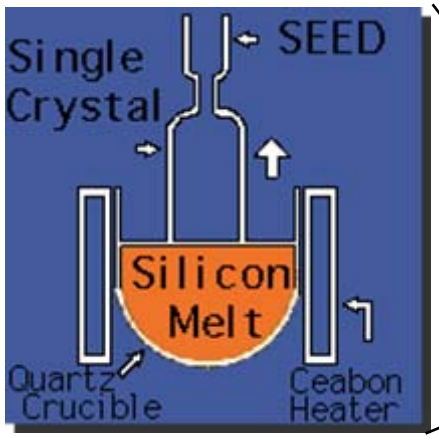


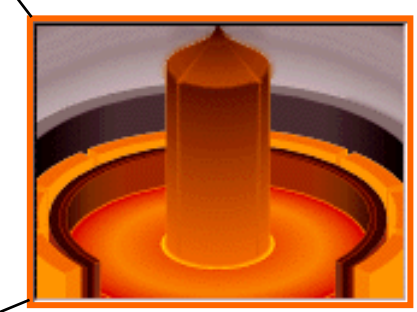
- **First ICs cost ~$120 and contained 10 transistors ($12/transistor), today's microprocessors cost ~$500 and contain 500,000,000 transistors ($0.000001/transistor)**
  - **If this cost scaling was applied to the automobile industry a $100,000 Porsche 911(turbo) would now cost < 1 cent**

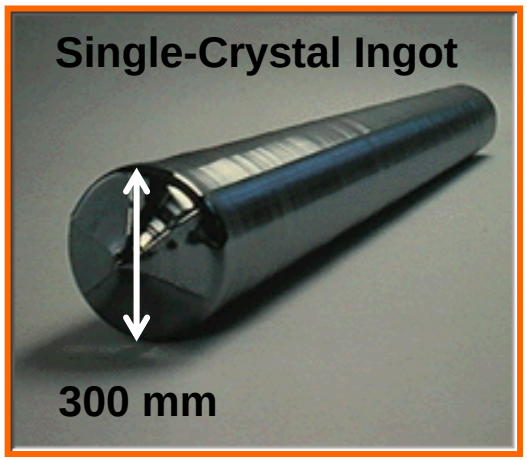
Silicon – The Material Enabling the IC

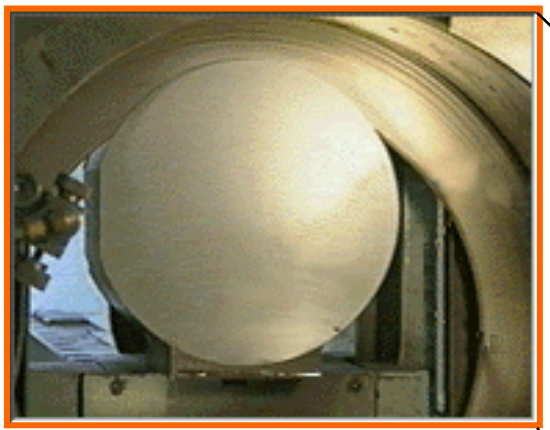
(Semiconductor Wafer Preparation)

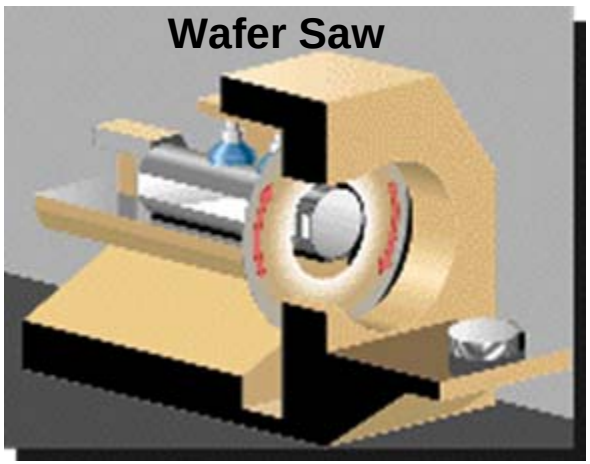






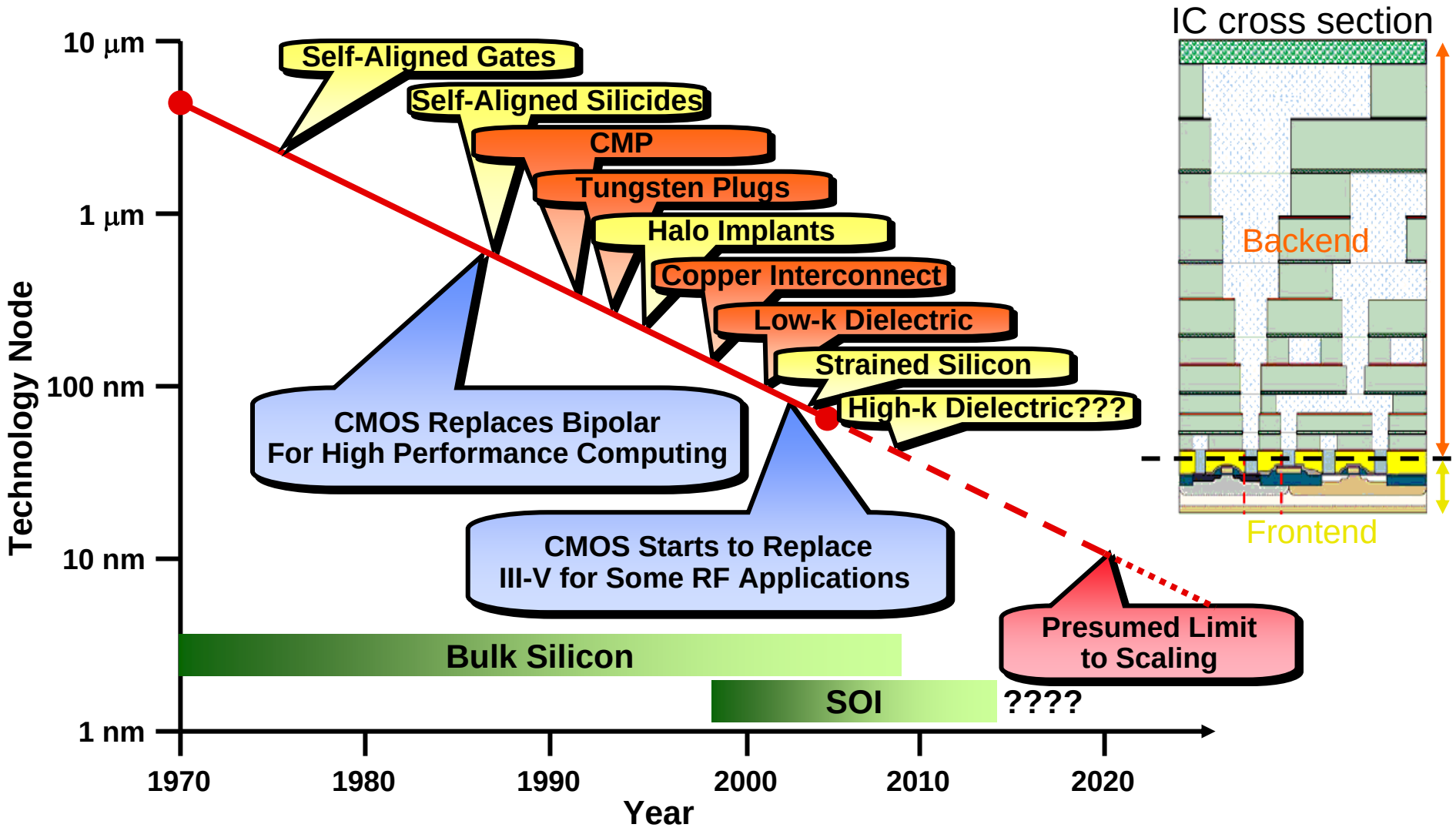






Silicon's Oxide (SiO_2) is a KEY attribute of this material's success

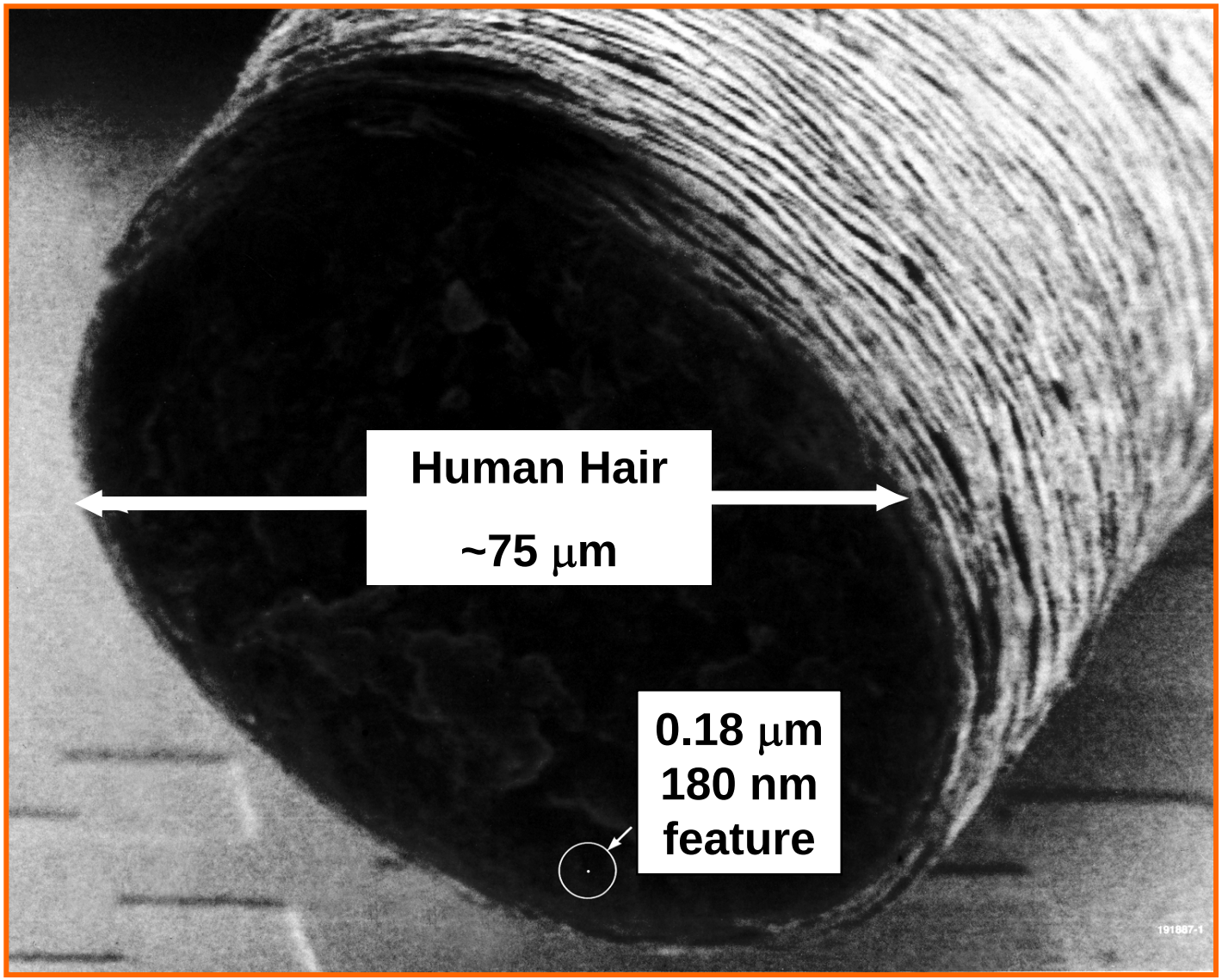
35 Years of CMOS Scaling and Process Improvements



Drivers Behind Moore's Law

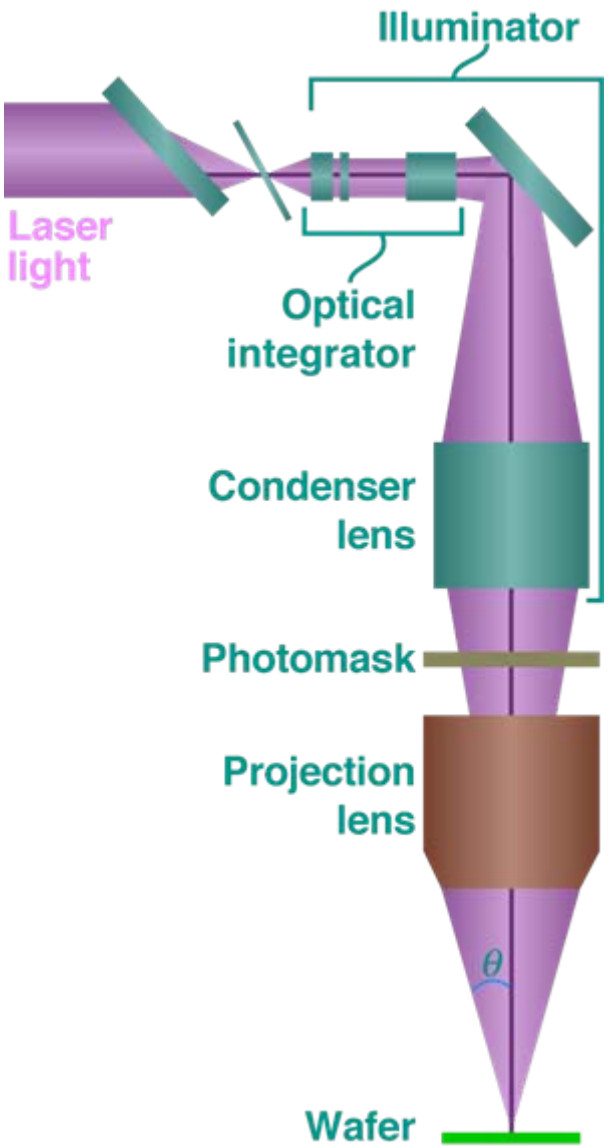
- Smaller feature sizes
  - Pack more features in given silicon area
    - Lower cost per function
  - Smaller transistors are faster
  - Smaller transistors and wires consume less energy
- Bigger chips
  - More functions on one chip reduces packaging and integration costs, reduces power, improves reliability
- Bigger wafer sizes
  - More chips per wafer; wafer processing cost for bigger wafers rises more slowly than number of transistors/wafer
- Manufacturing know-how
  - Faster machines, higher yields, better tool utilization
- More clever device, circuit, and process design
  - Pack more in a given area, even for a given feature size
  - "Equivalent scaling": next generation performance through improved process/materials: SiGe, SOI, strained silicon

Shrinking Feature Size….



~40,000 (65-nm node) transistors could fit on cross-section

Lithographic Tools



~10'

- **Current State of the art (>$25 M)**
  - 65 nm resolution
  - λ = 193 nm
  - 0.93 NA ($n \sin\theta$)
  - > 10^{13} pixels/wafer
  - ~120 300-mm wafers/hour
  - Wafer & mask move 100's of mm/s during exposure

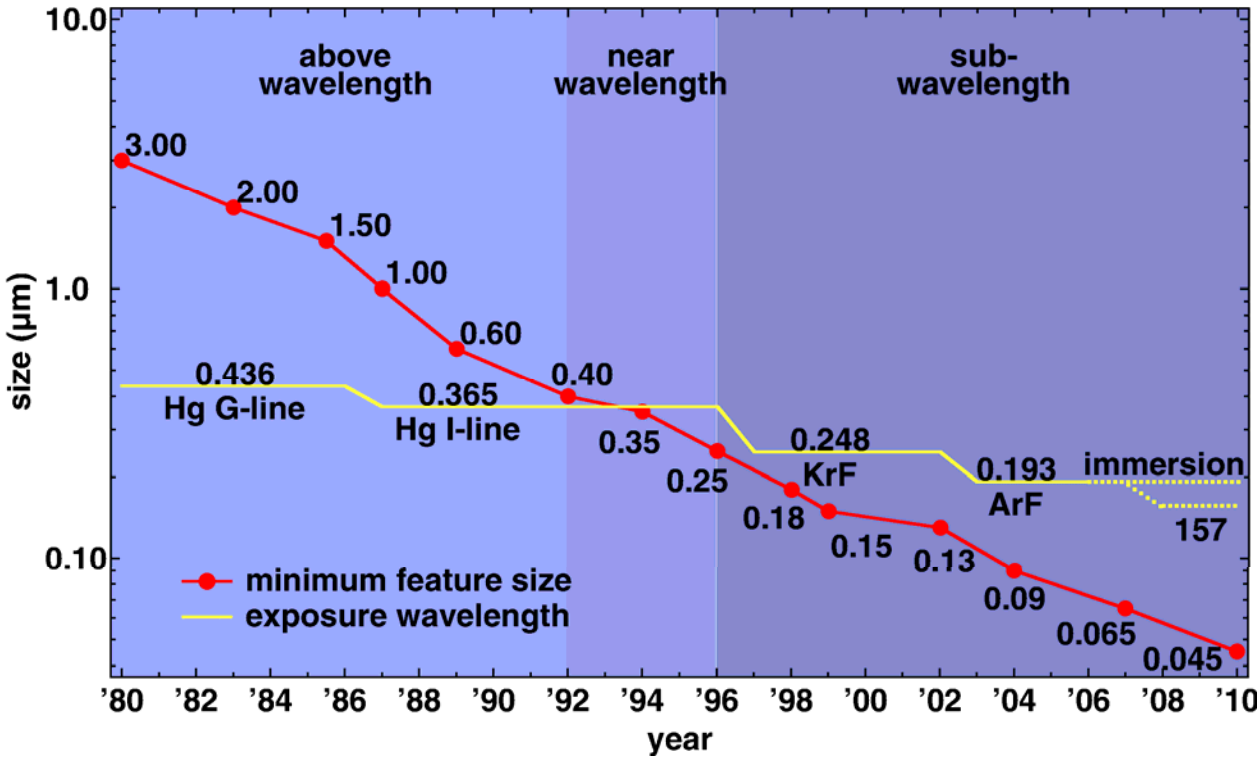
$$W \approx k_1 \frac{\lambda/n}{\sin\theta}$$

Optical Lithographic Resolution

- **Rayleigh criterion for resolution *W***

$$W = k_1 \frac{\lambda / n}{\sin\theta}$$

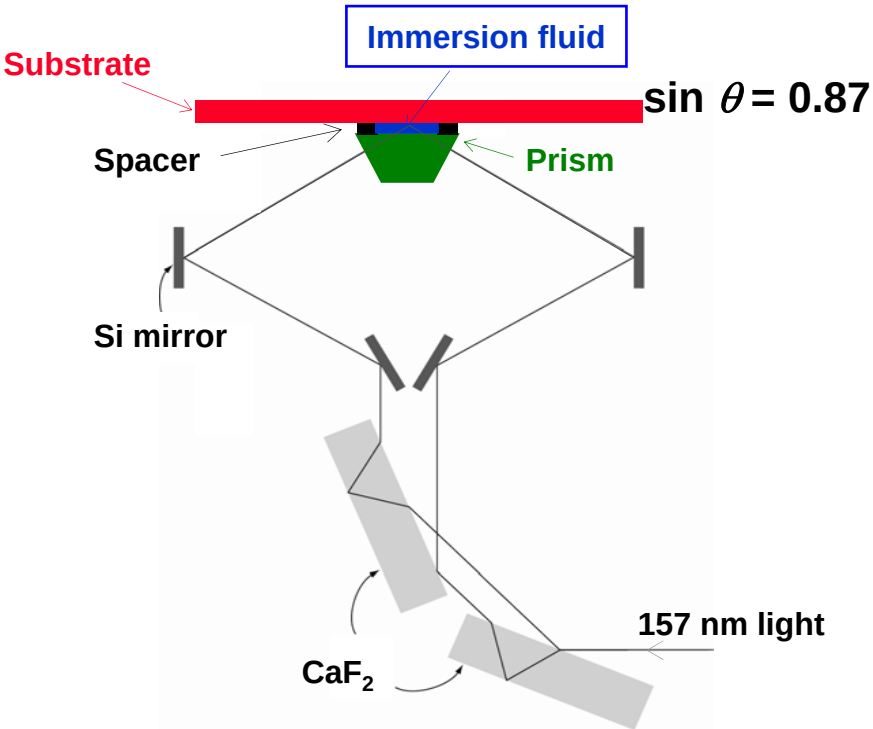
- **30x improvement in resolution over 25 years**
  - **λ from 436 nm to 193 nm**
  - **sin θ from 0.35 to 0.93**
  - **k_1 from 0.6 to 0.35**
  - ***n* from 1 to 1**
- **Now approaching limits**
  - **λ limited by materials and sources**
  - **sin θ < 1**
  - **k_1 > 0.25**
  - ***n* ???**

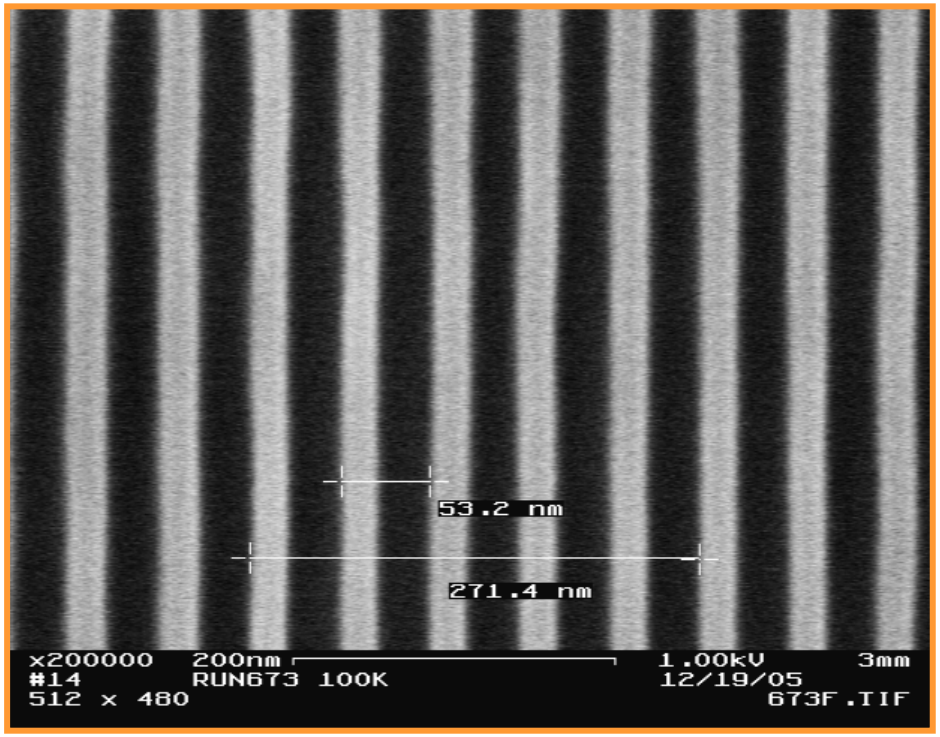


Slide Courtesy M. Switkes, MIT-LL

Liquid Immersion Interference
27-nm Half Pitch

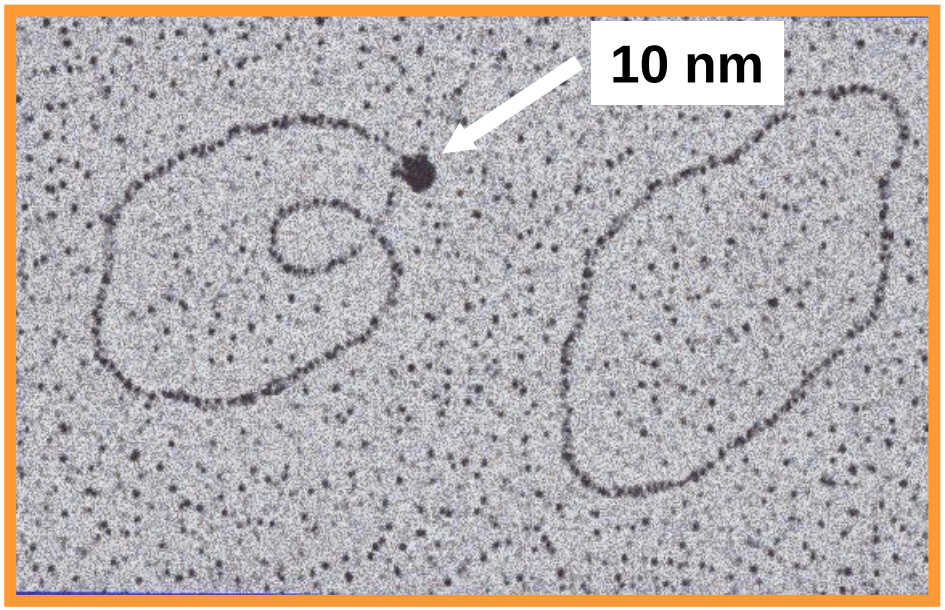
- **High-index fluids have been designed and synthesized (n_{157} = 1.50)**
- **Enable coupling of light from prism to wafer**
  - **No need for solid contact – liquid gap of 2 μm is used**

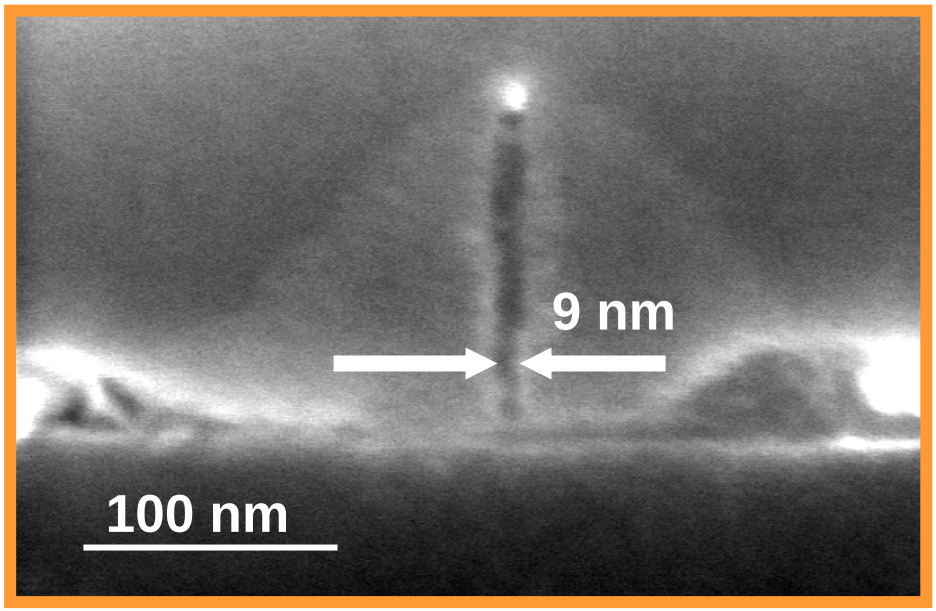




Slide Courtesy M. Rothschild, MIT-LL

Optical Lithography at the Nanometer Level





10 nm gold particle attached to Z-DNA antibody. (John Jackson & Inman. Gene [1989] 84, 221-226)

9-nm polysilicon gate on ultra-thin SOI fabricated at MIT-LL using 248-nm PSM optical lithography *(2001)*

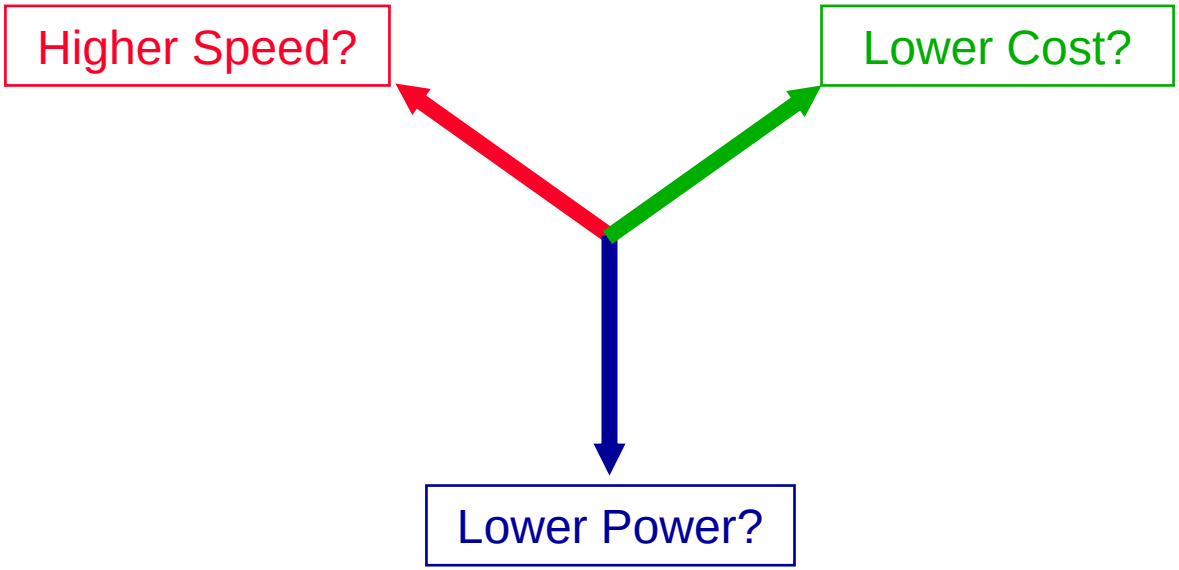
It is likely that we can pattern the smaller feature sizes needed to maintain CMOS scaling….

But will the devices work?

Prognosis For Moore's Law Benefits

- **Historically, CMOS scaling has resulted in *simultaneous improvements* in cost per function, circuit (and system) speed, power consumption, and packing density**

- **Will continued scaling give us the same benefits?**



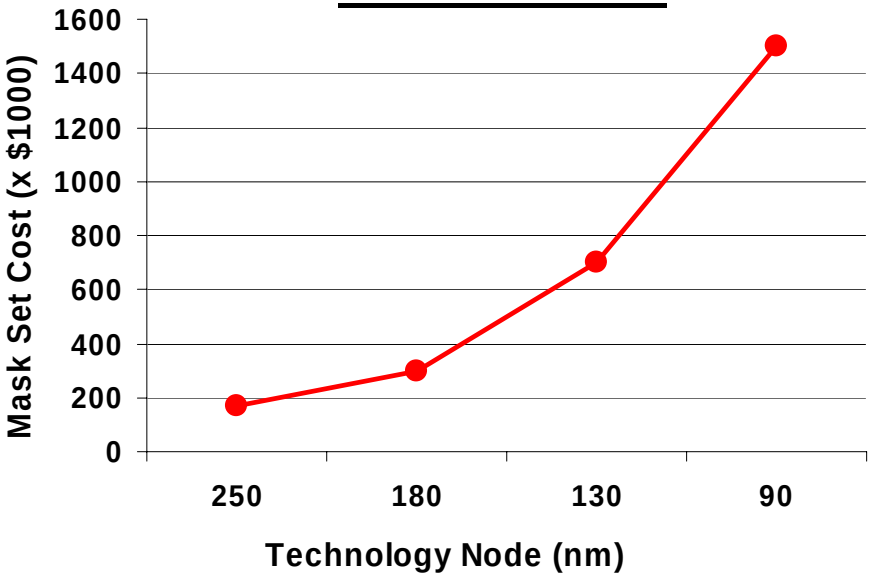
Lower Cost
Prognosis For Moore's Law Benefits

Past

- Scaling (s) increases components per unit area as s^2
- Wafer size increase gives more chips per wafer

⇨Increasing cost of equipment outweighed by huge increase in number of transistors made per wafer

Mask Set Cost



Future Issues

- Skyrocketing equipment costs…Today's state-of-the-art production facilities cost ~4 billion dollars
- NRE (e.g. >$1M mask sets) and productivity issues favor large volume production of "generic" components
- Increasing consolidation/pooling of fabrication resources and use of Taiwanese "Super Fabs" TSMC and UMC (China and India next?)

Lower Power
Prognosis For Moore's Law Benefits

Past

- Supply voltage (V) scales as 1/s
- Capacitance (C) scales as 1/s
- Energy per op scales as CV2 ∝ 1/ s3

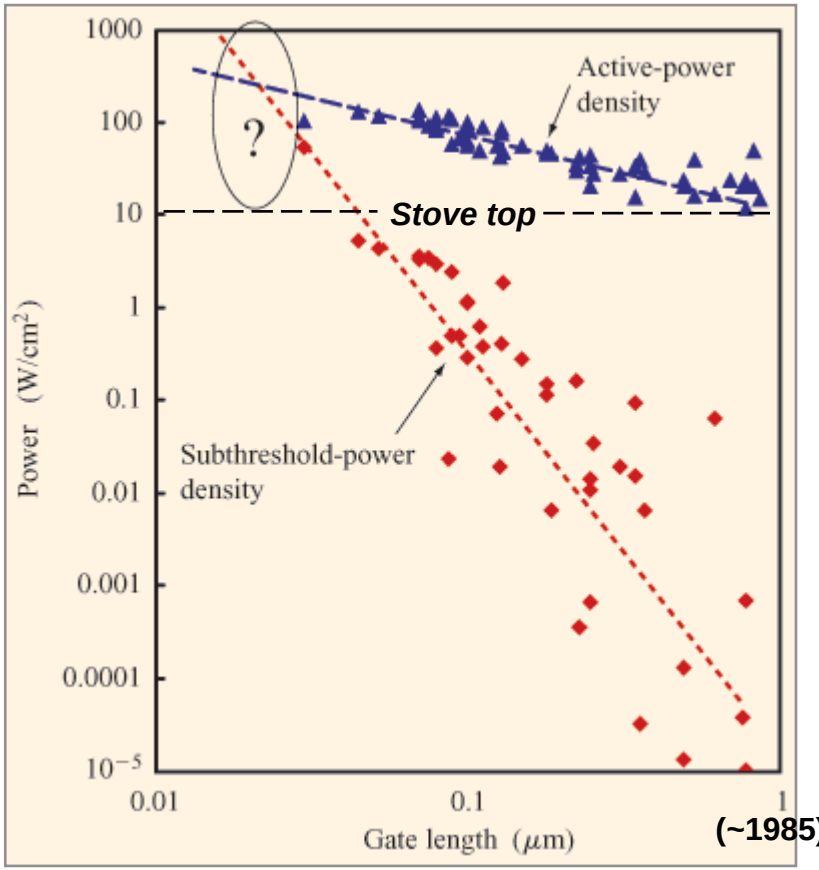
⇨ Voltage scaling from 5V to 1V accounted for 25X reduction in power, just by itself

Future Issues

- Power supply voltage only projected to drop 2X over next 15 years (1.0 to 0.5 V)
- Subthreshold device operation?

⇨ Scaling energy per op is critical to long endurance battery powered systems and to supercomputers (getting power in and heat out)

Passive and Active Power vs Gate Length

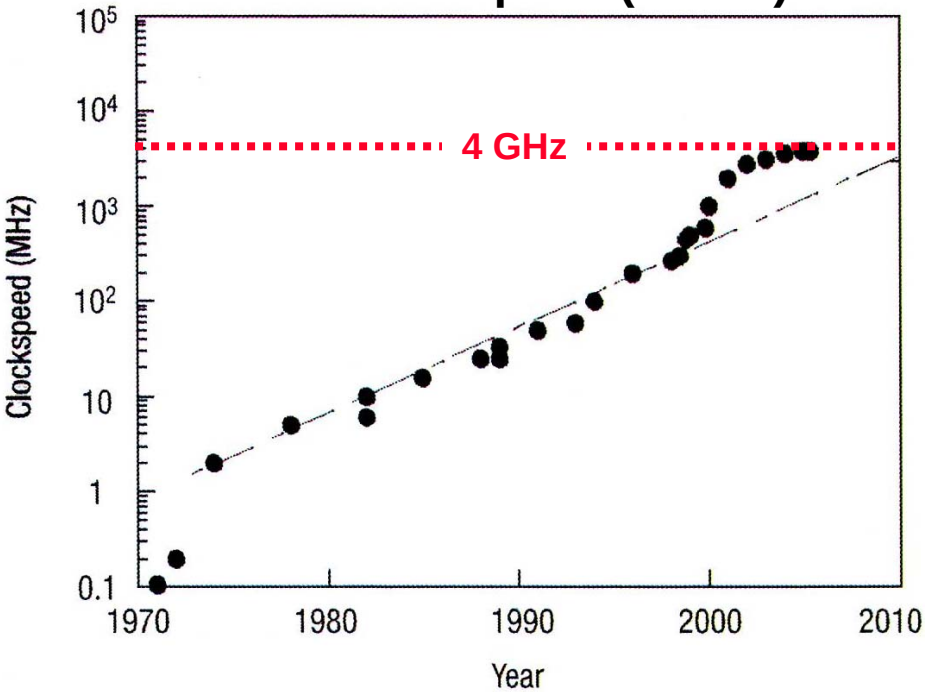


(~1985)

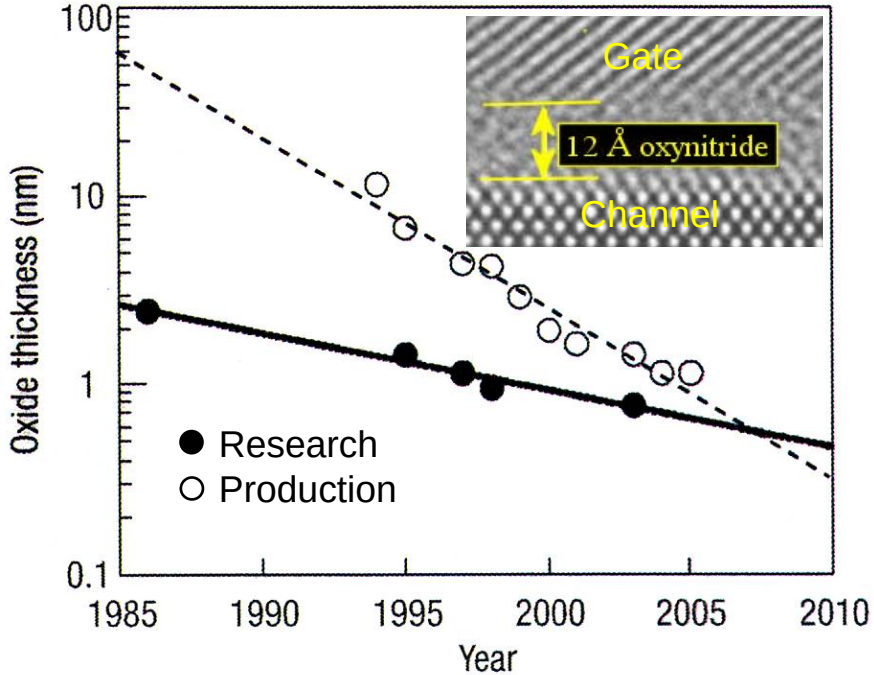
E. J. Nowak, IBM J. Res. & Dev., Vol. 46, No. 2/3, p. 173

Higher Speed
Moore's Law in Trouble

Processor Speed (INTEL)*



Gate Oxide Dielectric*

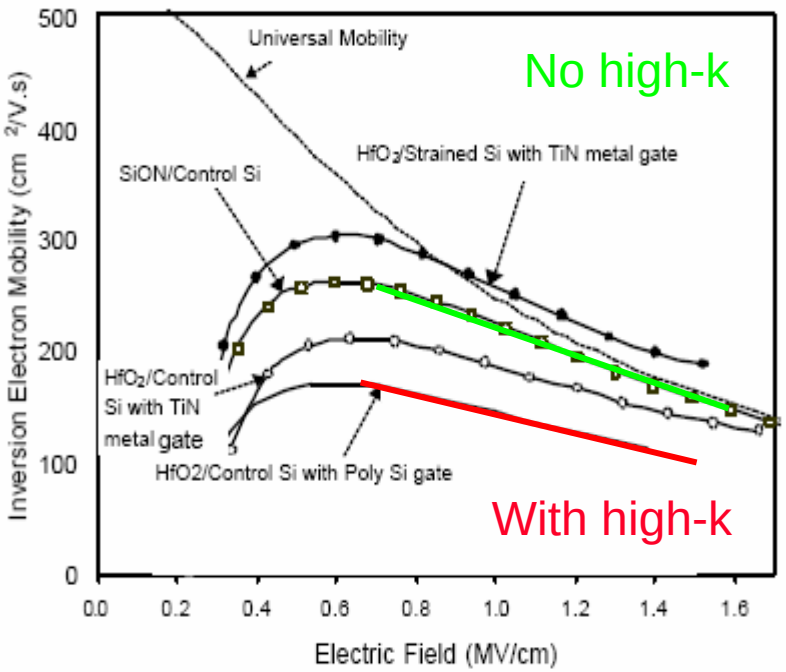


- **CPU speed has stalled for the first time in 35 years, with no processor able to break through the "4-Ghz barrier"**
- **Why?...Gate oxide scaling has stopped at Tox~1.2nm in 2003, at the 90-nm technology node (~3-4 monolayers)**
  - **Only heroic integration efforts, such as use of strained-Si, have made small dents in the CPU speed barrier**
  - **Need a workable High-k gate dielectric in order for performance scaling to continue**

**D. A. Muller, Nature Materials V 4, pg. 645 (2005)*

Future High Performance Device "frontend" Possibilities

- **Continue with Si CMOS. Some possible alternative silicon futures are:**
  - **CPU speed could be maxed out – future improvements will come from reduced cost and higher density and integration "multi-core" chips**
  - **High-k could save the day – if not tomorrow, maybe in 10 years**
    - **A perfect high-k gate dielectric will enable CPU speeds to increase until the next tunneling limit (source-to-drain) at the 10nm-node**
  - **Changes in device architecture could take the pressure off the gate oxide, and CPU speed will continue to advance at a slower rate**
    - **FDSOI and FinFET lets T_{si} scale instead of T_{ox}**

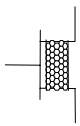


Intel - components research (IEDM2003)

Future Possibilities (Cont'd)

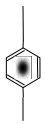
- **A future with transistors, but without silicon:**
  - **Germanium-based devices**

    Improved mobility, at the expense of many other semiconductor properties
  - **Carbon-based devices. Several flavors:**



Carbon nanotubes: Have better device properties than Si, but are very difficult to integrate (thus far)

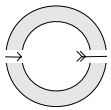
Graphite devices: Difficult to turn off



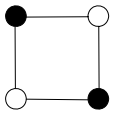
Molecular devices: Have not been demonstrated to work better than Si

Future Possibilities (Cont'd)

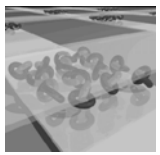
- **A future without transistors:**



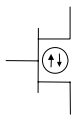
  - **Josephson-junction-based logic**
    - **Demonstrated and works, but at 4K**
    - **Real speed and power advantages unclear**



  - **Quantum Computation**
    - **Can't execute traditional code, even theoretically**
    - **But can solve Schrödinger's equation blazingly fast, and factor very large numbers**

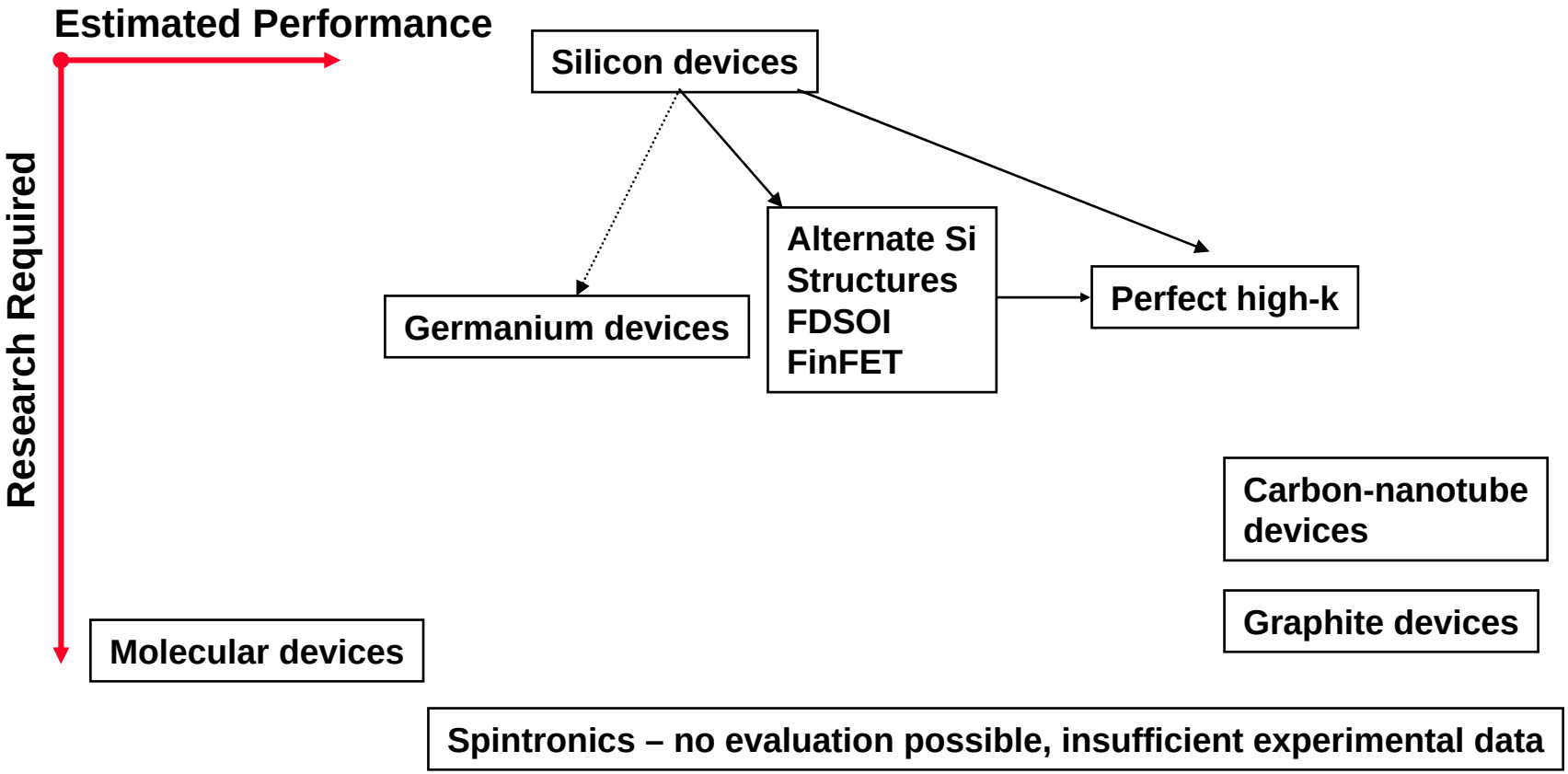


  - **Cross Point Arrays – nanowire, molecular**
    - **Too simple for general purpose logic, if complexity is increased to meet logic constraints the result is a transistor**



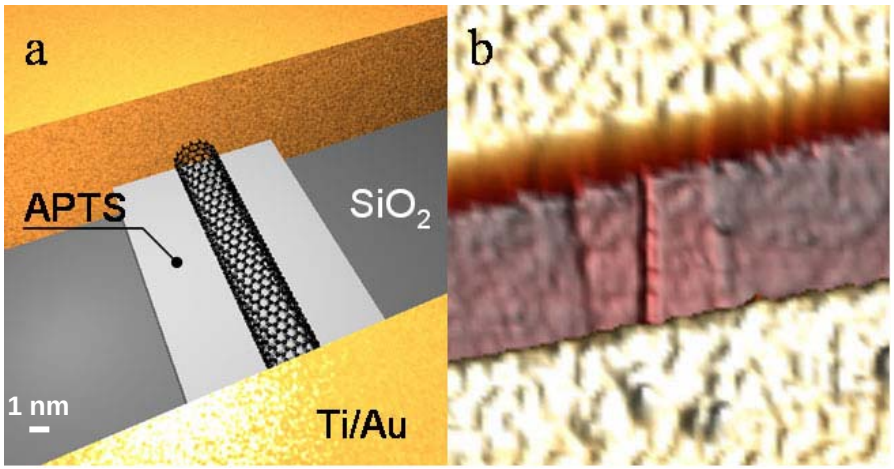
  - **MEMS, protein, spin logic – too early to evaluate**

Potential Technology Roadmap

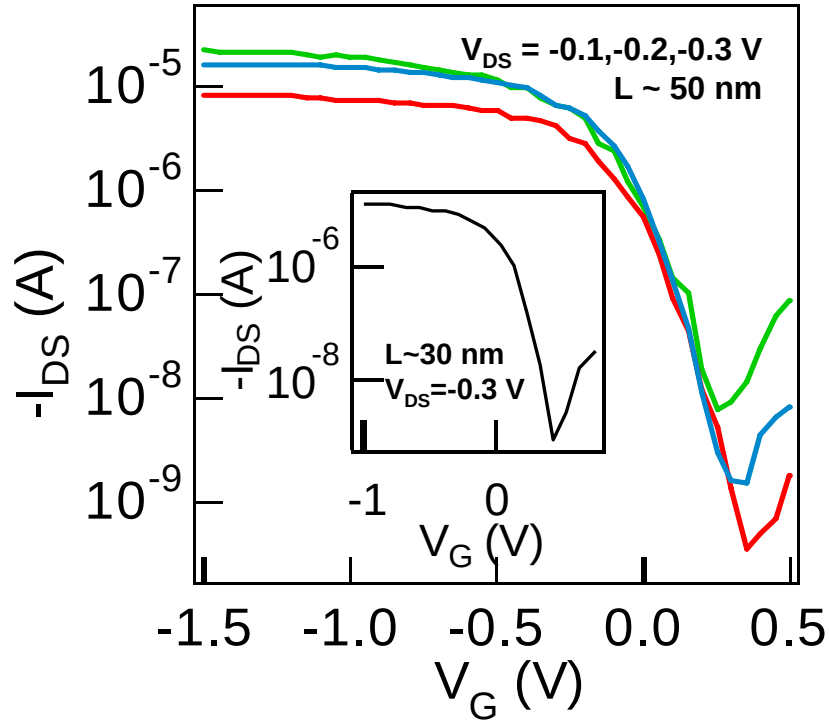


Possible global directions for high performance logic technology in the next 20 years considered in this study, and graphical summary of their evaluations when possible

Future Technology Highlights: Carbon Nanotubes (CNTs)



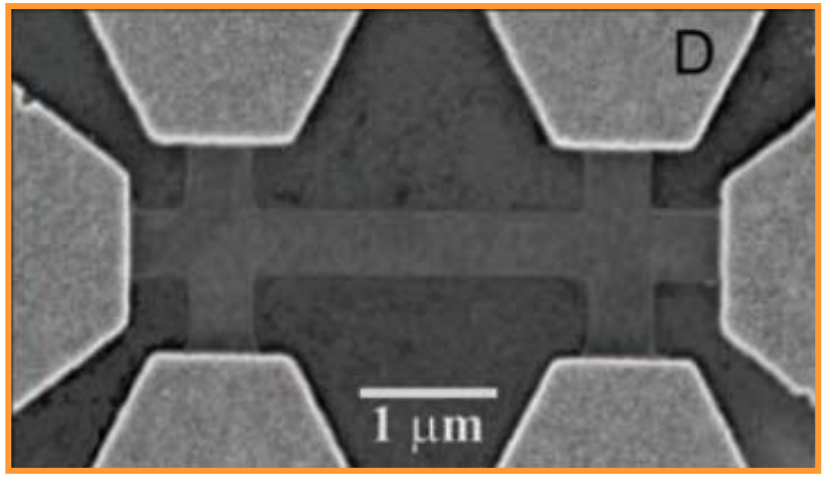
(Drawing and AFM from CEA website)

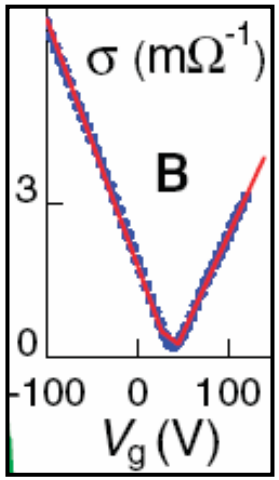


- **Example of experimental CNT device from Stanford**
  - **Features: metal gate, high-k dielectric, metal source/drain**
  - **High performance: 10x Si device of same geometry**
- **Putting tubes were they are needed is a problem**

REF: A. Javey, et al. Nano Lett, 2004.

Future Technology Highlights
Thin Graphite - Graphene



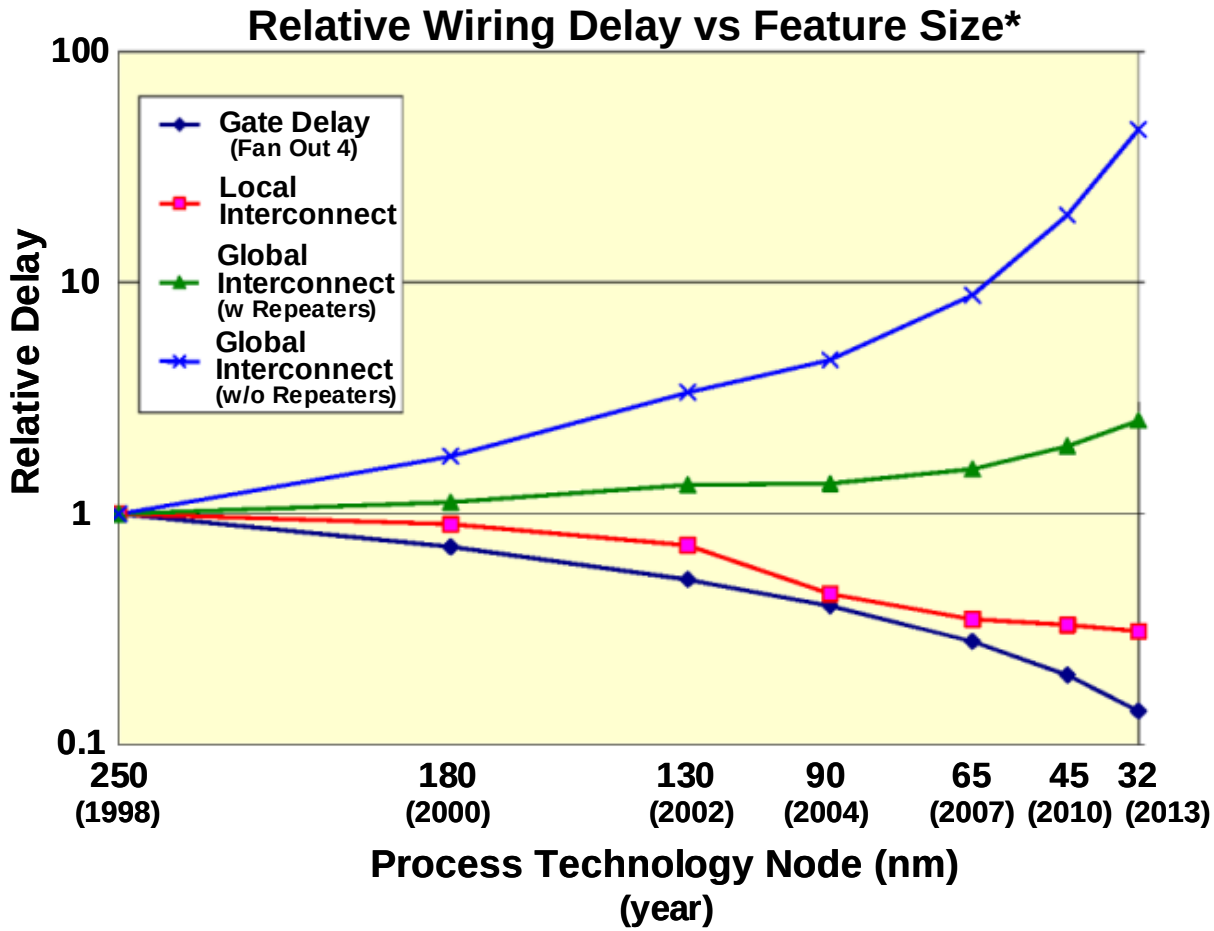


REF: K.S Novoselov et al., Science, V. 306, 22 October 2004, p. 666

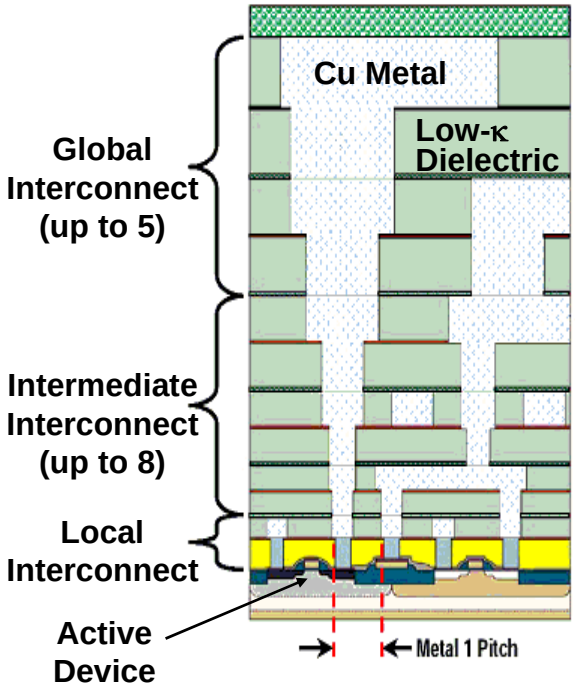
Few monolayer graphite device SEM and electrical characteristics at T=70K

- **Graphite has high mobility of >10,000 cm^2/Vs (~15x Si)**
- **Graphite is a semi-metal (semiconductor with band-gap of 0eV)**
  - **Difficult to turn off, a fundamental challenge**
- **Proven planar techniques could be used in fabrication**
  - **Planar geometry of devices eliminates majority of integration difficulties of carbon nanotubes**
- **MIT-LL has begun to explore this material system**
  - **Leveraging layer transfer, materials, and microelectronic fabrication expertise at the Laboratory**

The Integrated Circuit Interconnect "backend" Challenge

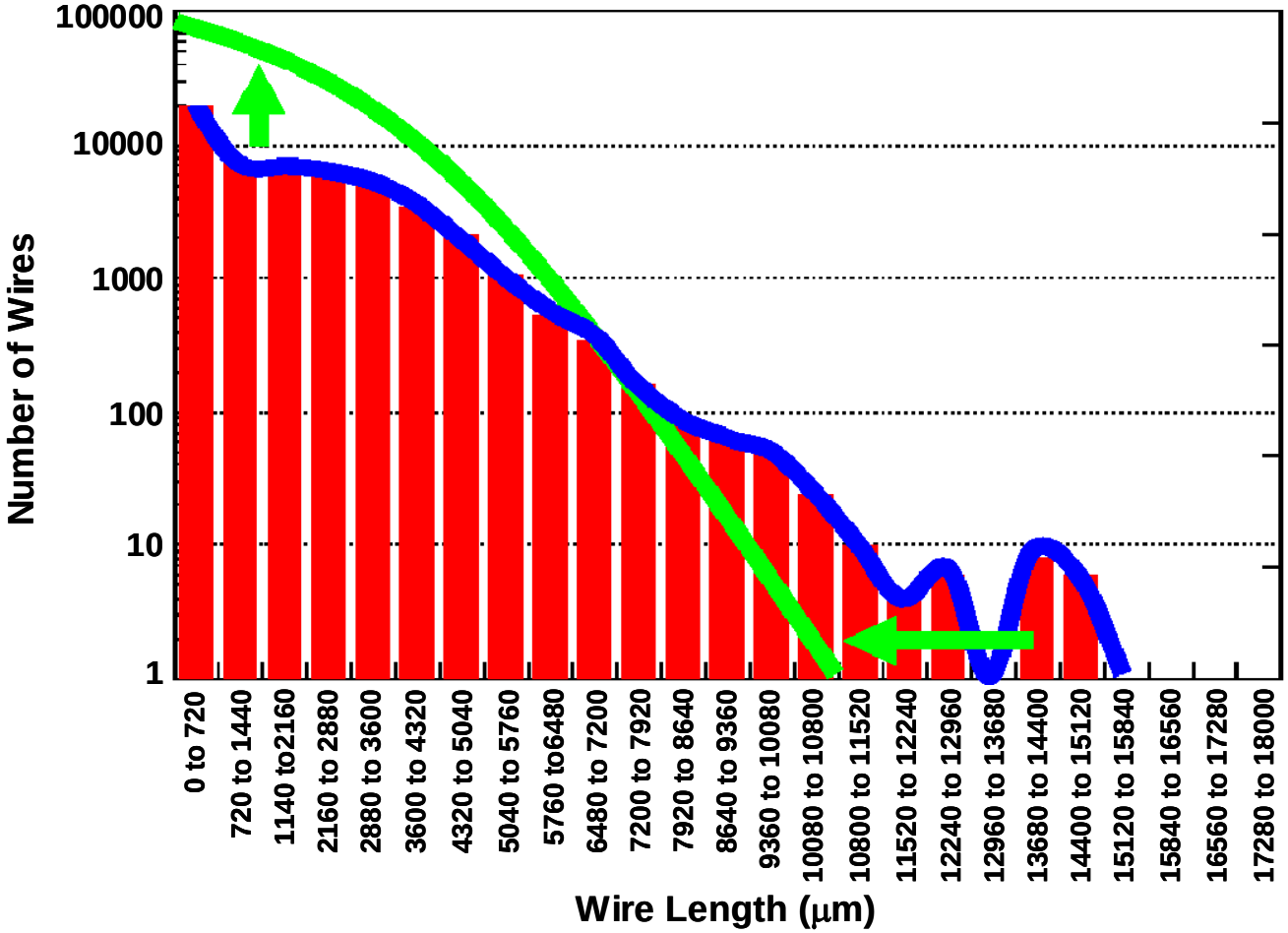


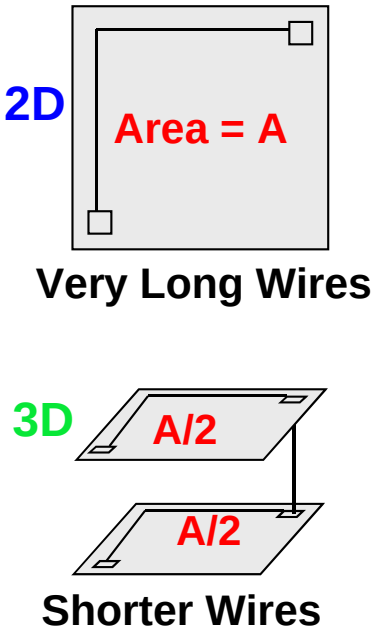
Typical Process Cross-Section*



From 2005 International Technology Roadmap for Semiconductors (ITRS)

Wire Length Distribution in 90 nm Node IBM Microprocessor*

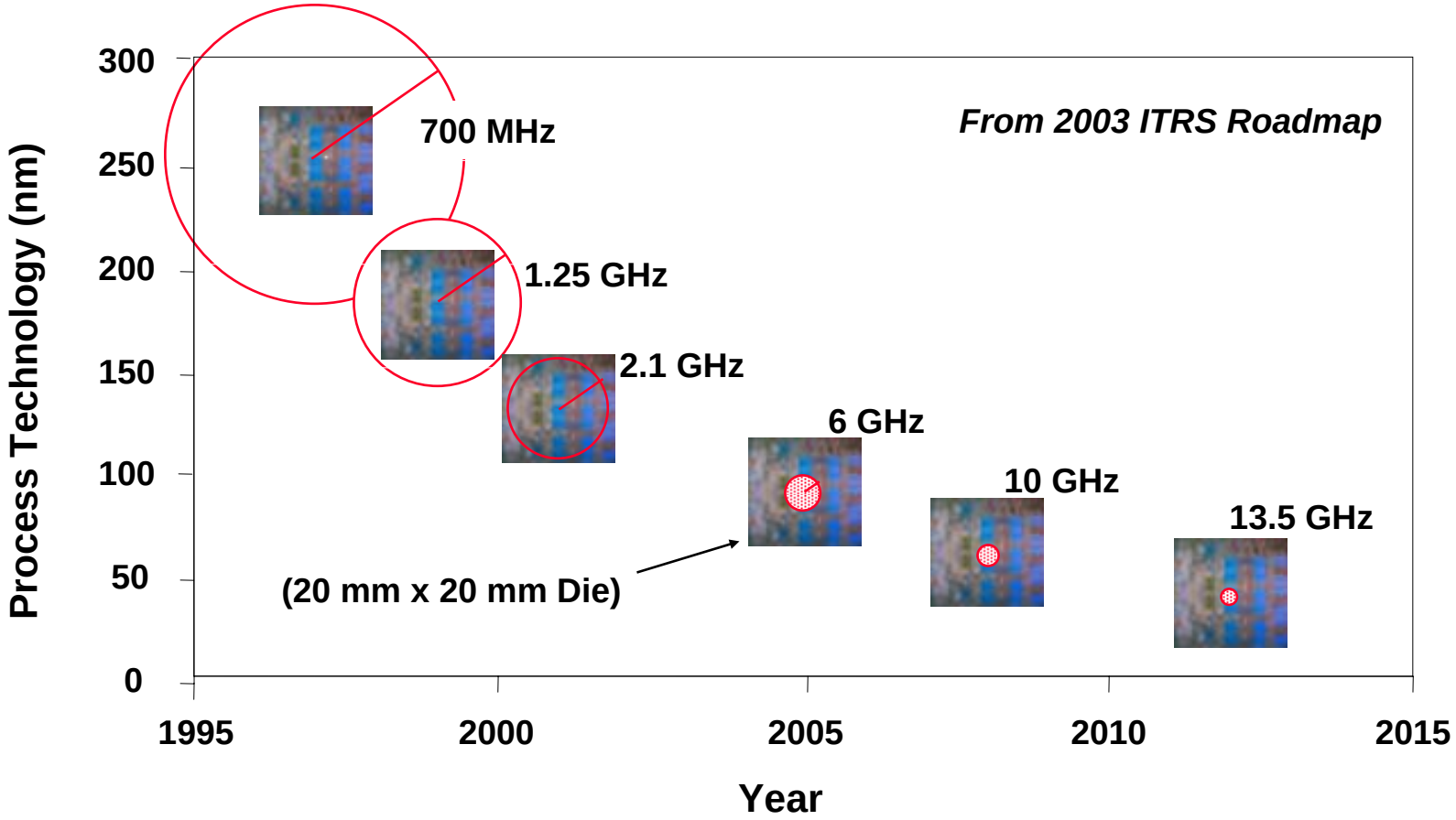




- >50% of active power (switching) dissipation is in microprocessor interconnects
- >90% of interconnect power is consumed by only 10% of the wires

*After K. Guarini IBM Semiconductor Research and Development Center

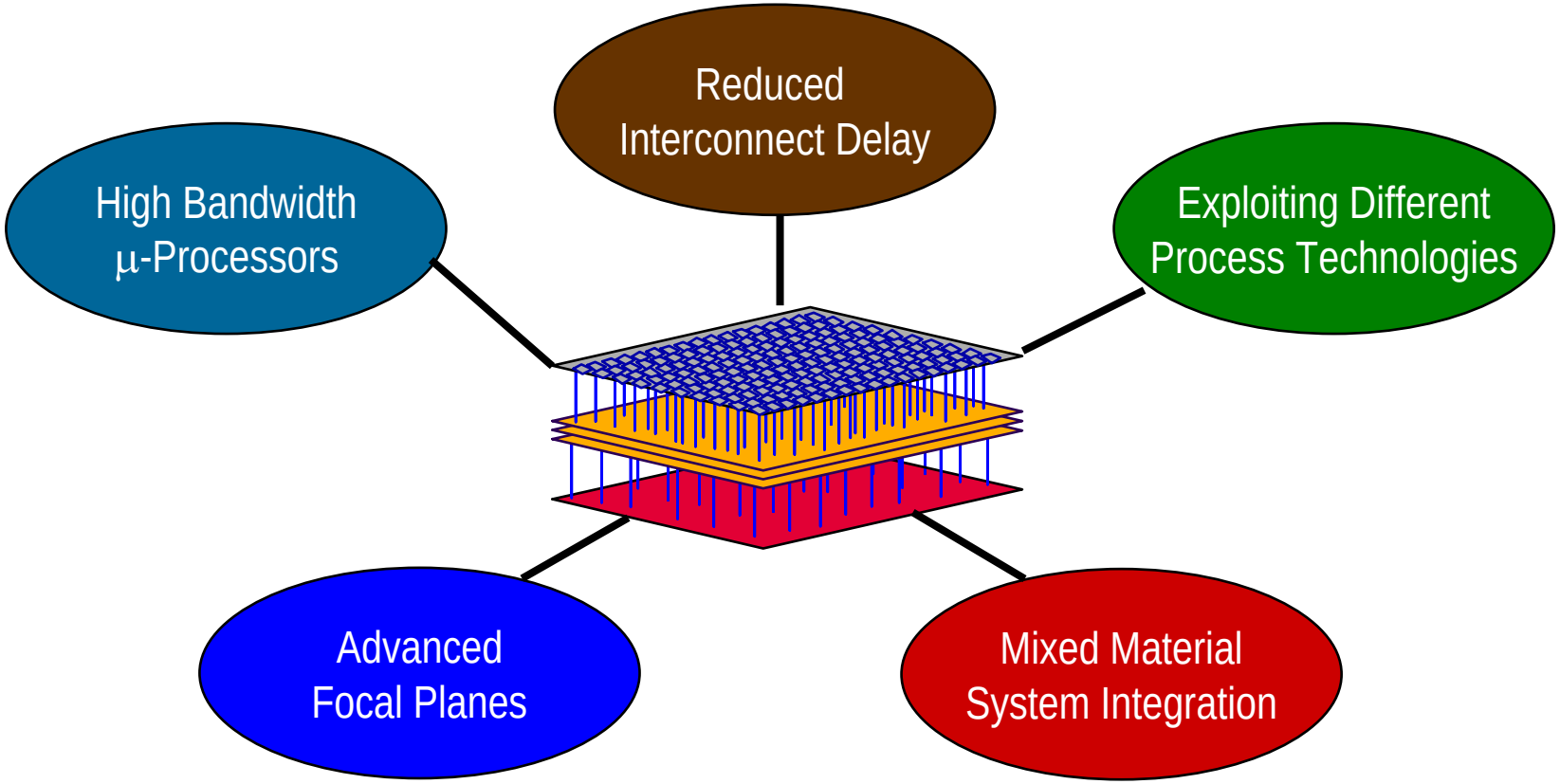
Range of Wire in One Clock Cycle*



- 3D Integration increases accessible active devices

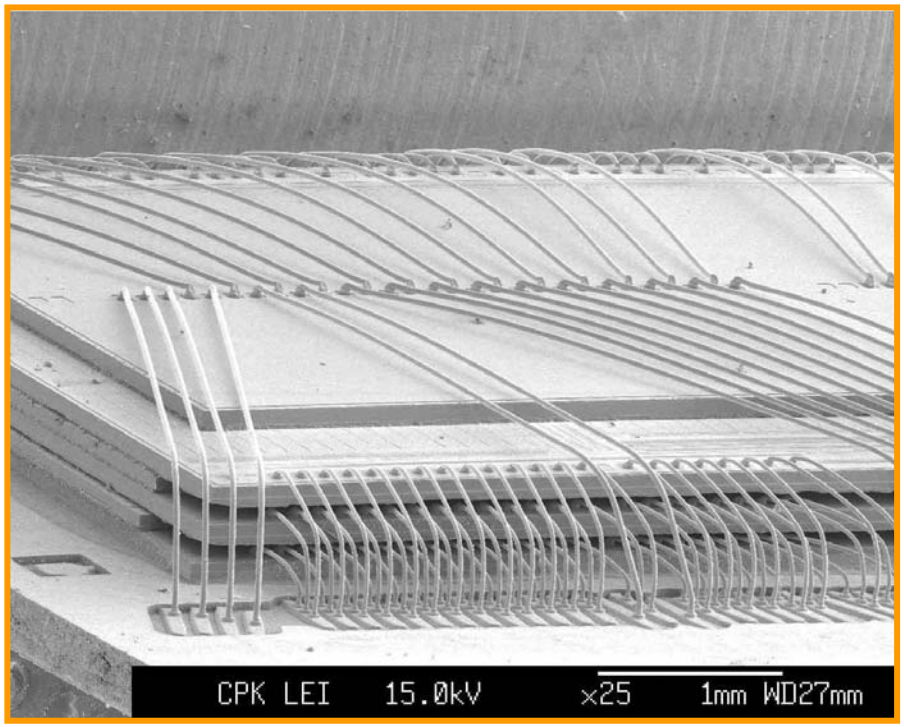
*After S. Amarasinghe, MIT Laboratory for Computer Science and Artificial Intelligence

Motivation for 3-D Circuit Technology



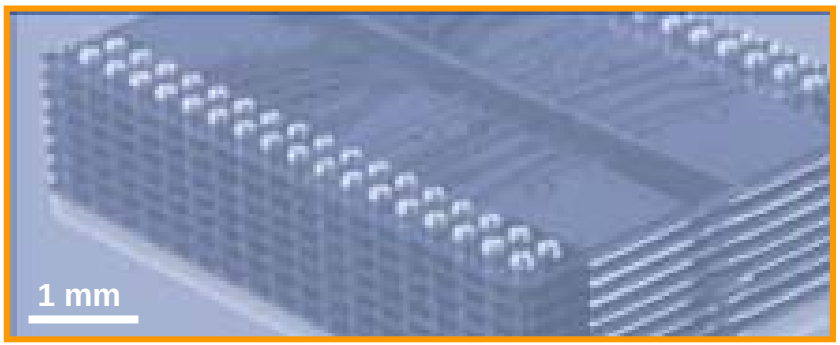
Pad-Level "3D Integration"
Die Stacking

Stacked-Die Wire Bonding



ChipPAC, Inc.

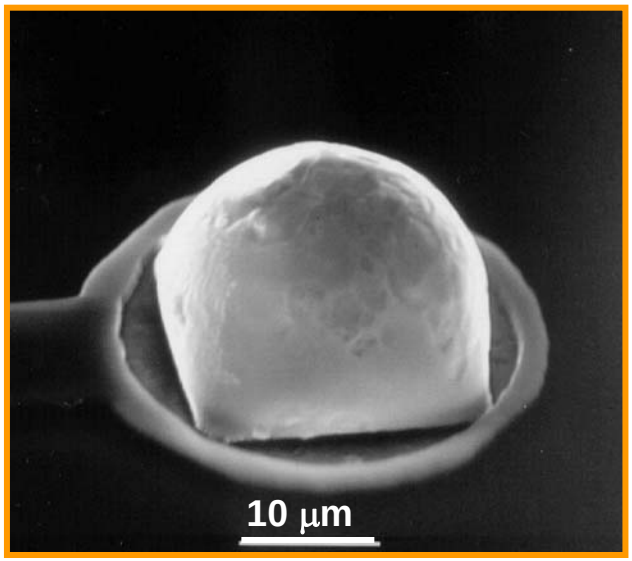
Stacked Chip-Scale Packages



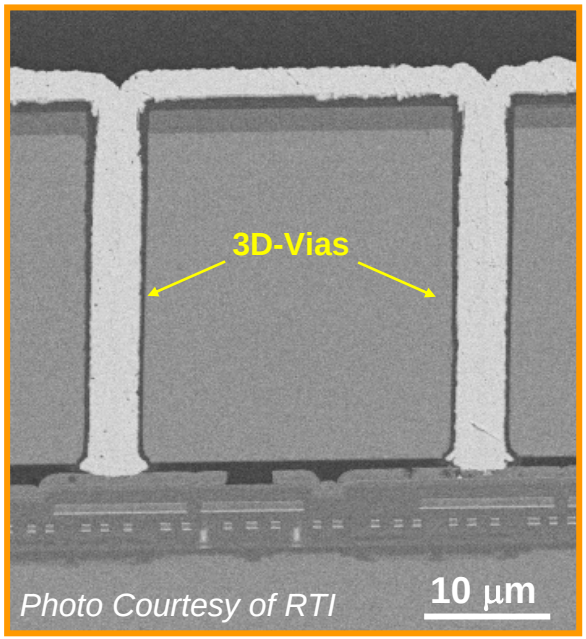
Tessera, Inc.

In Production!

Approaches to High-Density 3D Integration
(Photos Shown to Scale)



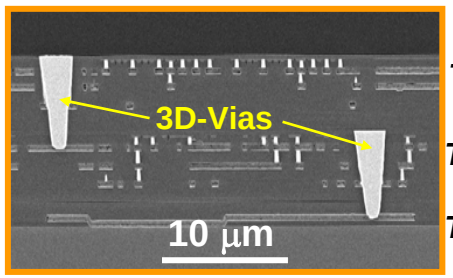
Bump Bond used to flip-chip interconnect two circuit layers



Tier-1

Tier-2

Two-layer stack with insulated vias through thinned ***bulk*** Si



Tier-3

Tier-2

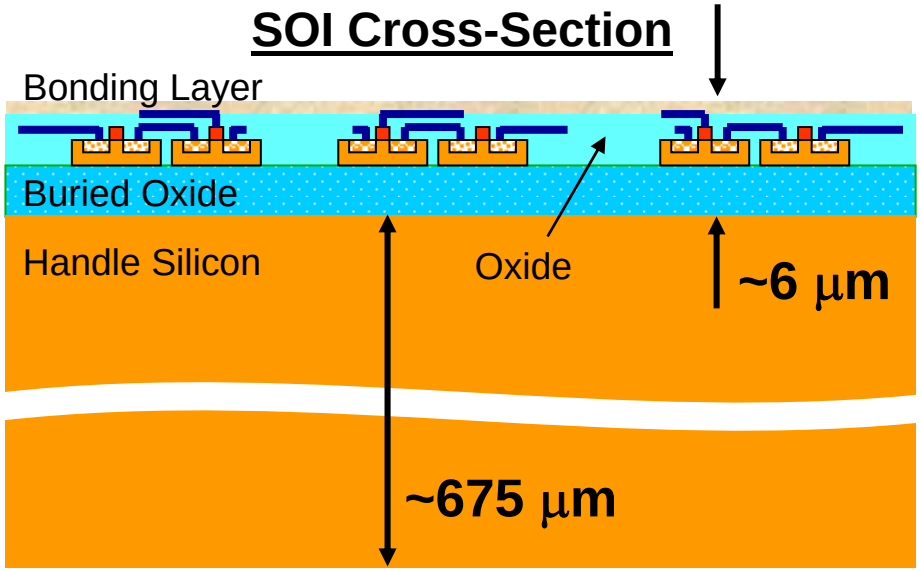
Tier-1

Three-layer circuit using MIT-LL's SOI-based vias

Advantages of Silicon-on-Insulator (SOI) for 3-D Circuit Integration

- The electrically active portion of an integrated circuit wafer is < 1% of the total wafer thickness

- Buried oxide layer in SOI provides ideal etch stop for wafer thinning operation prior to 3D integration



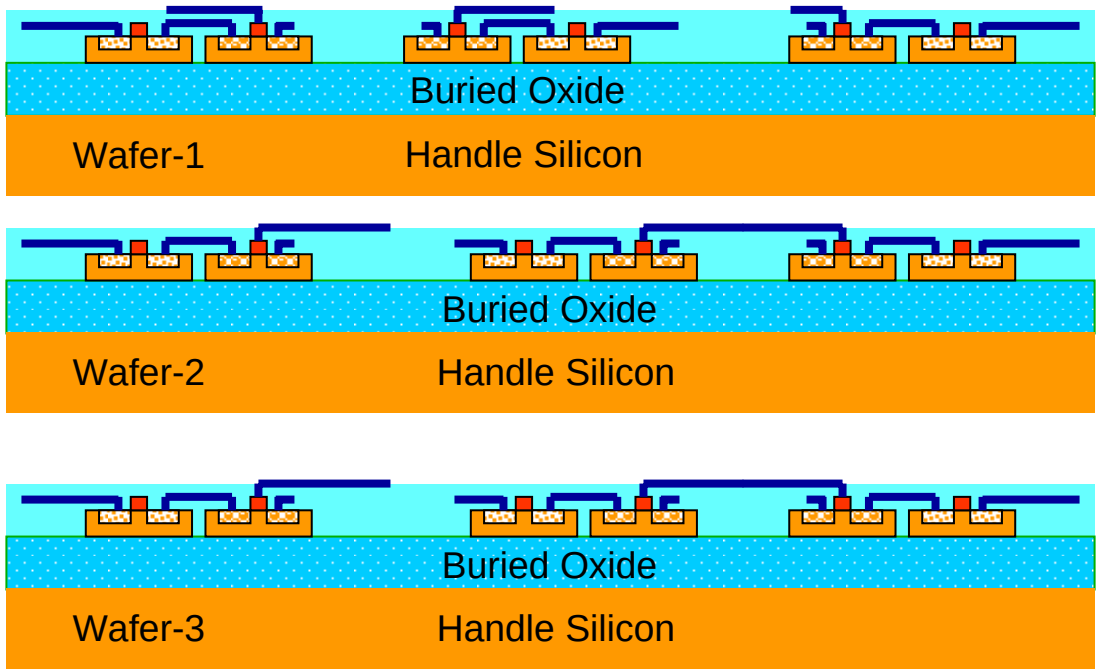
- Full oxide isolation between transistors allows direct 3D via formation without the added complexity of a via isolation layer

- SOI's enhanced low-power operation (compared to bulk CMOS) reduces circuit stack heat load

3-D Circuit Integration Flow-1

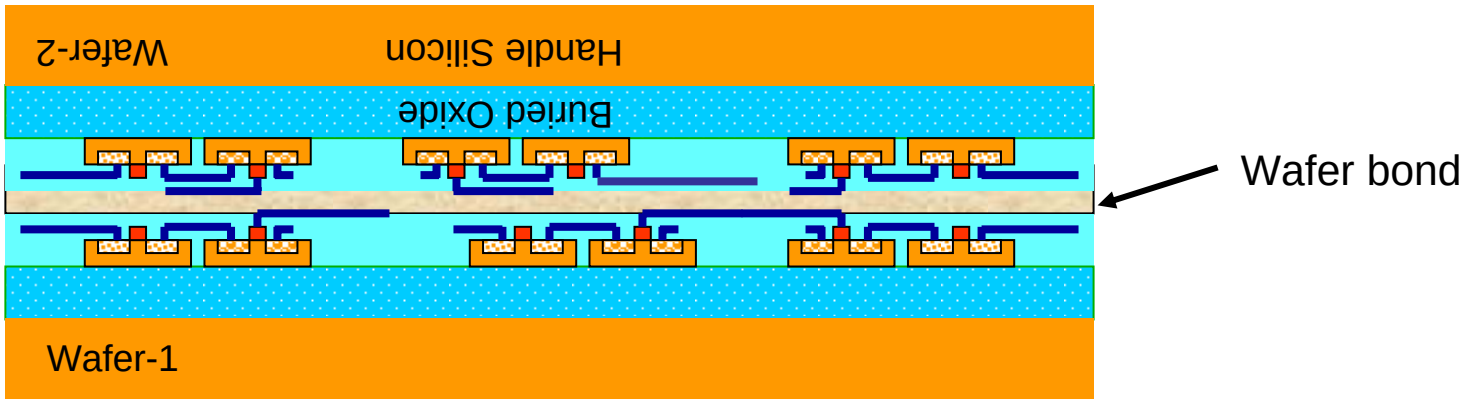
- **Fabricate circuits on SOI wafers**
  - **SOI wafers greatly simplify 3D integration**
- **3-D circuits of two or more active silicon layers can be assembled**

Wafer-1 can be either Bulk or SOI

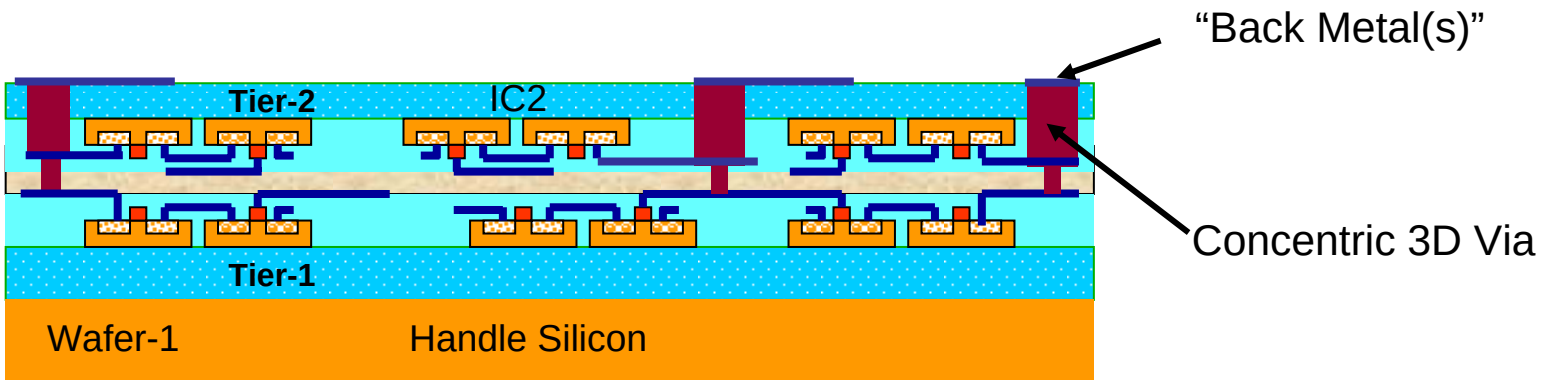


3-D Circuit Integration Flow-2

- **Invert, align, and bond Wafer-2 to Wafer-1**

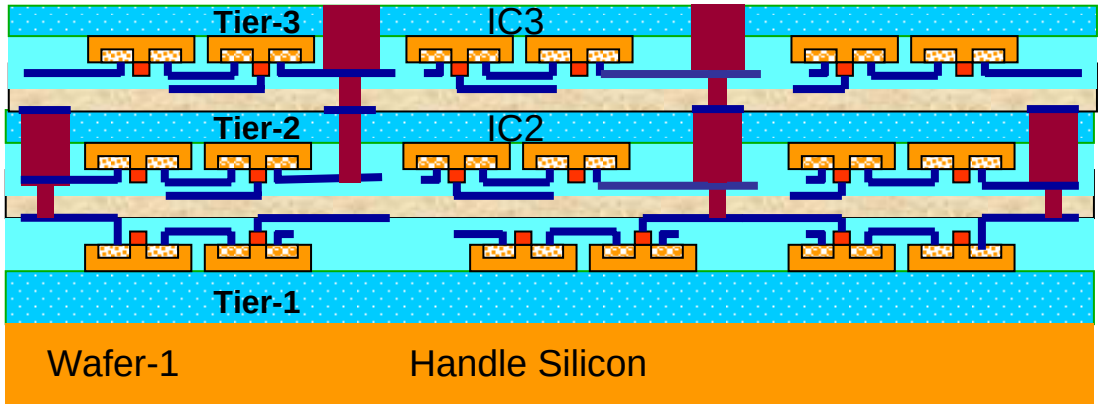


- **Remove handle silicon from Wafer-2, etch 3D vias, deposit and CMP damascene tungsten interconnect metal**

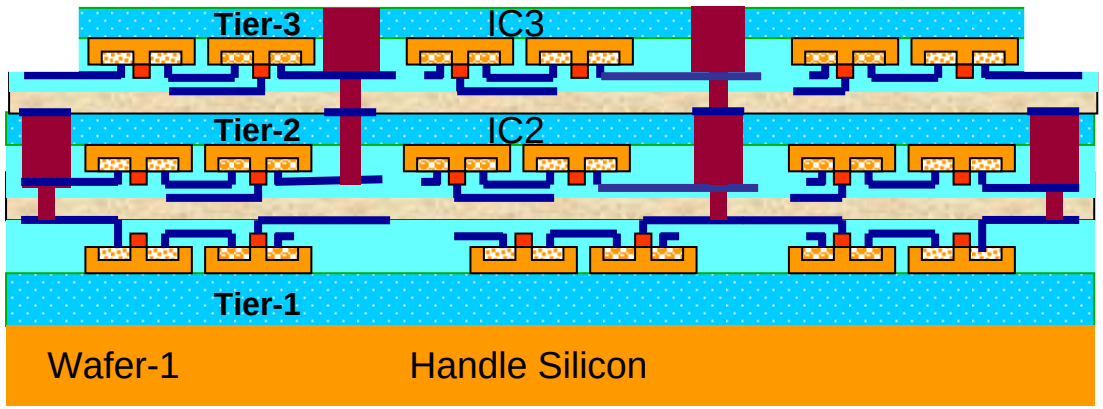


3-D Circuit Integration Flow-3

- **Invert, align, and bond Wafer-3 to Wafer-2/1-assembly, remove Wafer-3 handle wafer, form 3D vias**

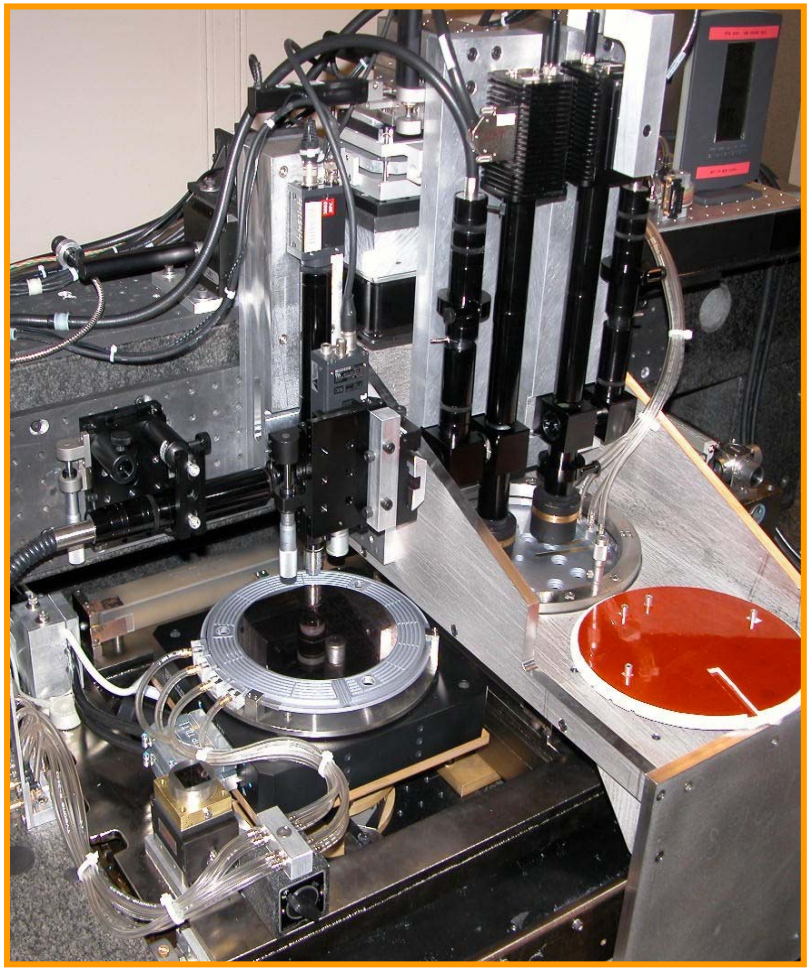


- **Etch Bond Pads**

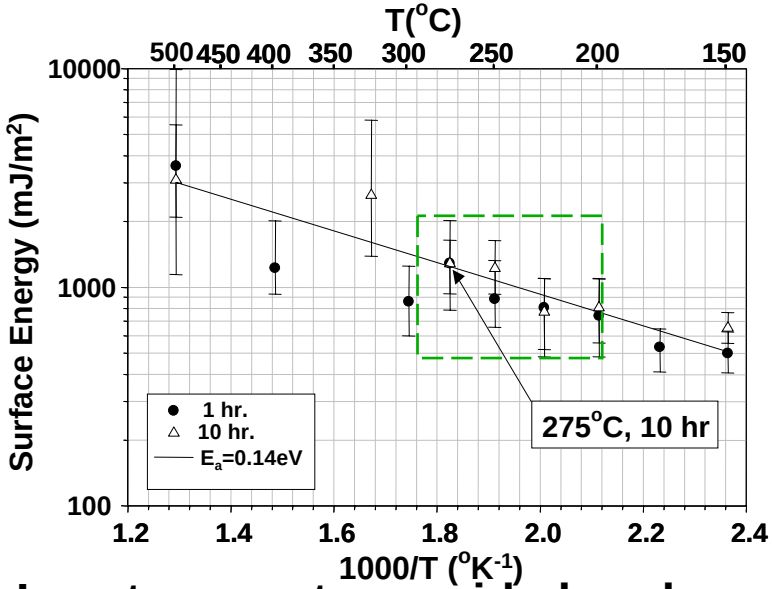


IEEE Trans. on Electron Devices, Vol. 53, No. 10, October 2006

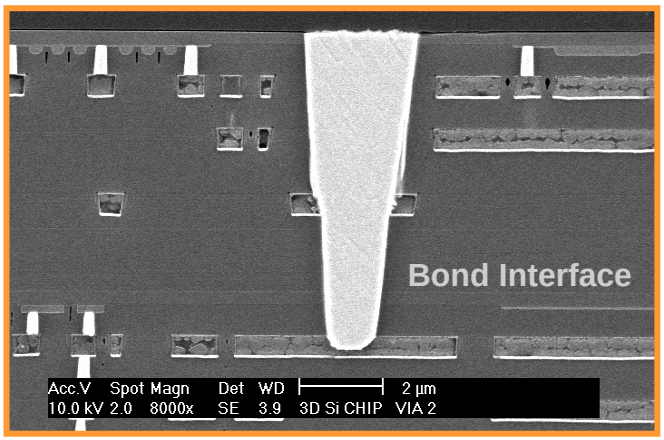
3D-Specific Enabling Technologies



Precision wafer-wafer alignment



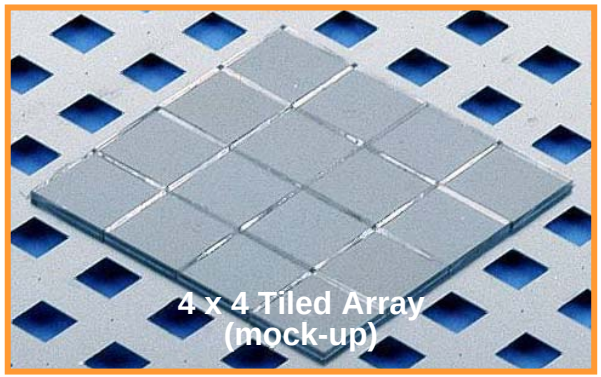
Low temperature oxide-bond process

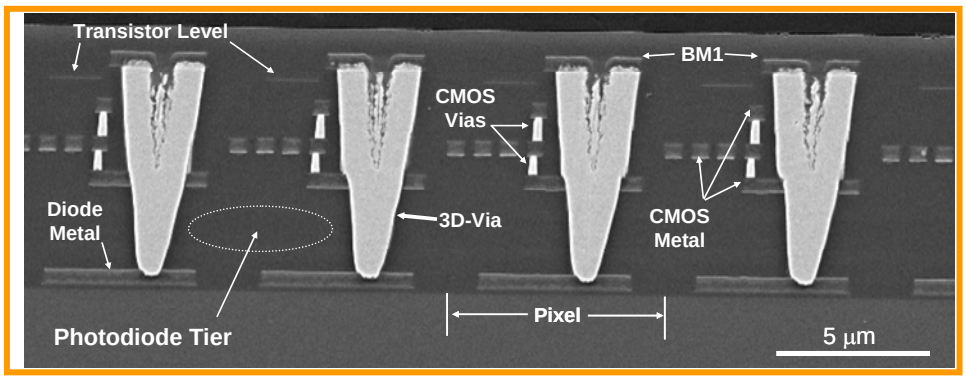


High-density 3D-Via

4-Side-Abuttable Mosaic Focal Planes

- **Tier-1: 100% fill-factor silicon photodetector layer**
- **Tier-2: CMOS address and readout layer**





Imager Cross-Section
(8 μm Pixel Pitch)

1024 x 1024 Image

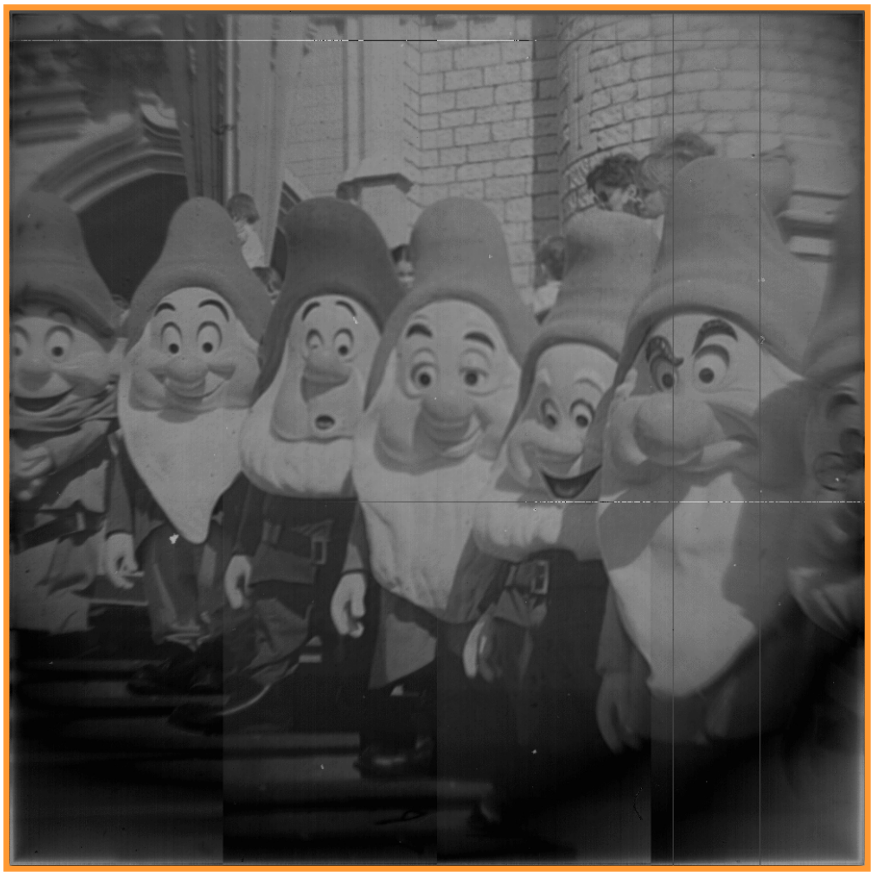
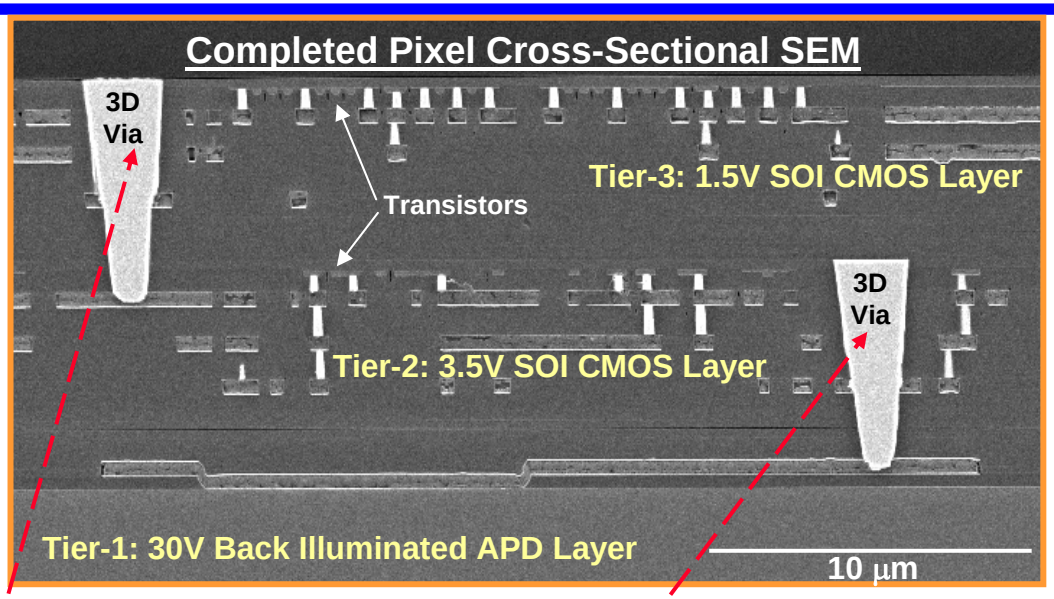


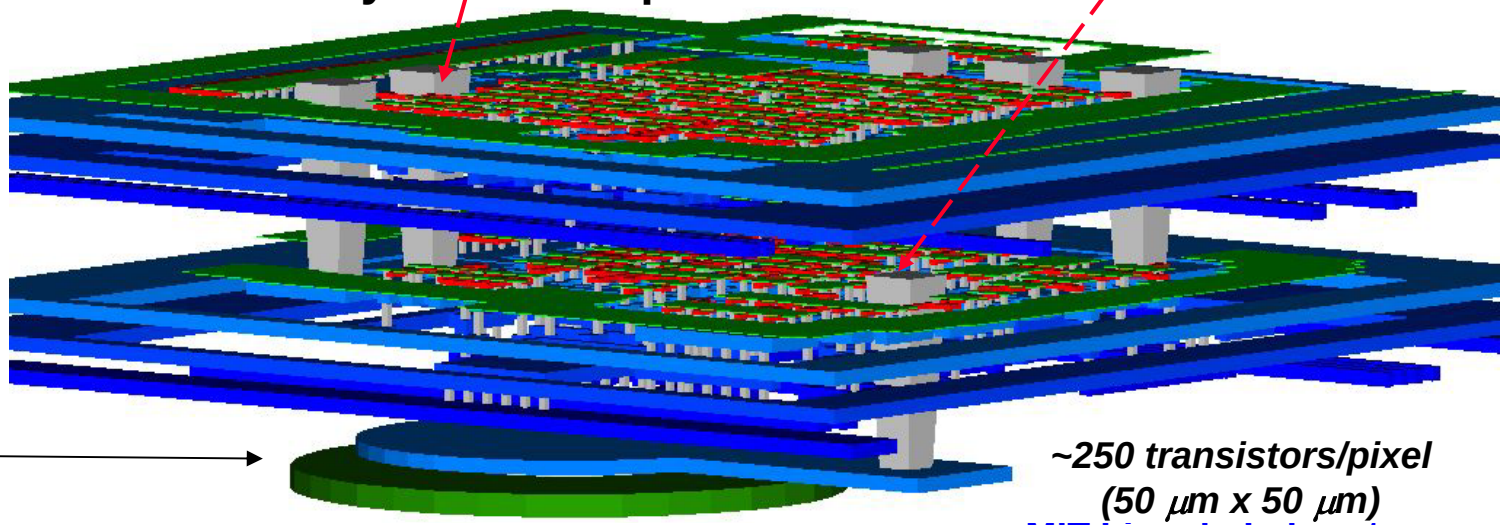
Image acquired at 10 frames/sec
(Background Subtracted, Pixel Yield > 99.9%, 3.8M transistors)

3D-Integrated, 3-Tier Avalanche Photodiode Focal Plane

- ***VISA*** **laser radar focal plane based on single-photon-sensitive Geiger-mode avalanche photodiodes**
  - **64 x 64 format**
  - **50-μm pixel size**



To-Scale Pixel Layout of Completed 3-tier Laser Radar Focal Plane



~250 transistors/pixel (50 μm x 50 μm)

Presented at 2006 ISSCC

First 3-D IC *Multiproject Run*

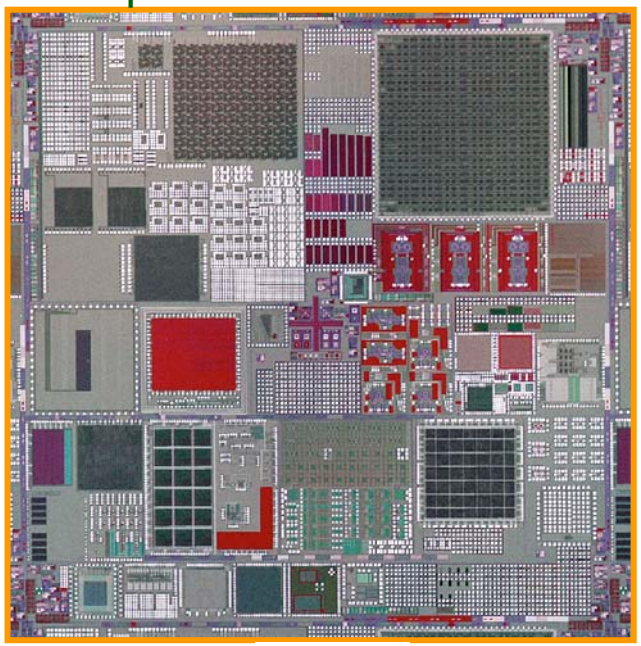
(Three 180-nm, 1.5 volt FDSOI CMOS Tiers)

- **Leverages MIT-LL's established 3D circuit integration technology**
  - **Low temperature oxide bonding, precision wafer-to-wafer overlay, high-density 3D interconnect**
- **Preliminary 3D design kits developed**
  - **Mentor Graphics – *MIT-LL*, Cadence – *NCSU*, Thermal Models – *CFRDC***
- **Design guide release 11/04, fab start 6/05, 3D-integration complete 3/06**

Concepts being explored in run:

3D FPGAs, digital, and digital/mixed-signal/RF
ASICs exploiting parallelism of 3D-interconnects
3D analog continuous-time processor
3D-integrated S-band digital beam former
Stacked memory (SRAM, Flash, and CAM)
Self-powered CMOS logic (scavenging)
Integrated 3D Nano-radio and RF tags
Intelligent 3D-interconnect evaluation circuits
DC and RF-coupled interconnect devices
Low Power Multi-gigabit 3D data links
Noise coupling/cross-talk test structures and circuits
Thermal 3D test structures and circuits

Completed 3DL1 Die Photo



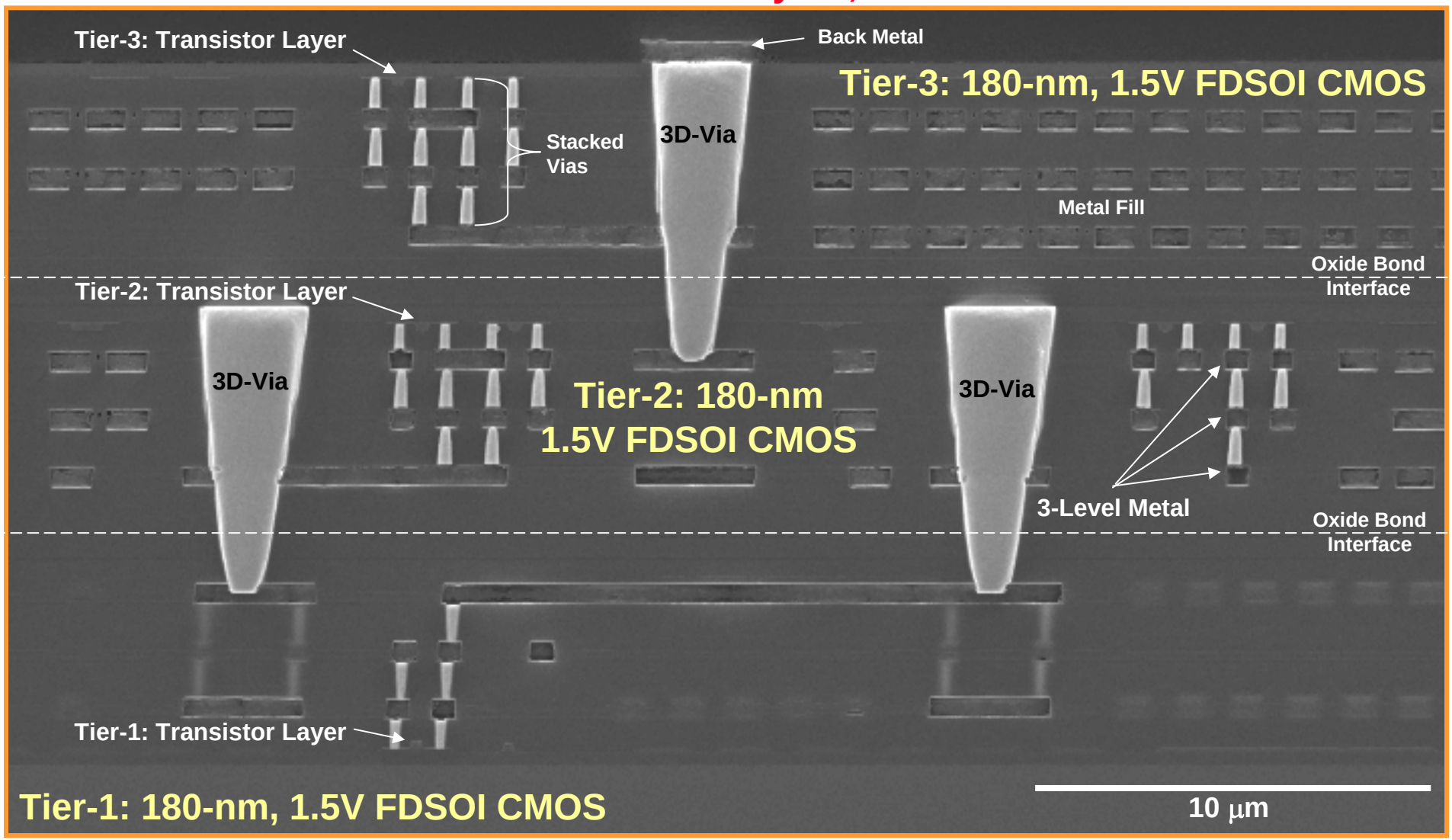
22 mm

3DL1 Participants (Industry, Universities, Laboratories)

BAE	Lincoln Laboratory	Purdue
Cornell	Maryland	RPI
Delaware	Minnesota	Stanford
HRL	MIT	Tennessee
Idaho	North Carolina State	UCLA
Johns Hopkins	NRL	Washington
LPS	Pennsylvania	Yale

Cross-Section of 3-Tier 3D-integrated Circuit
(DARPA 3DL1 *Multiproject Run*)

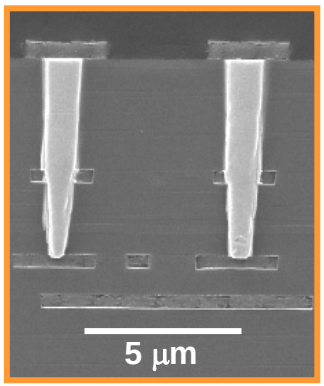
3 FDSOI CMOS Transistor Layers, 10-levels of Metal



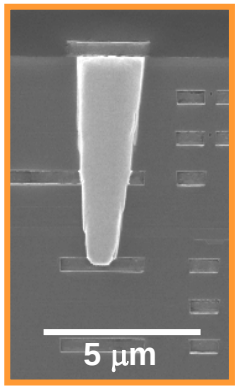
3D Technology Improvements
(DARPA 3DL1 *Multiproject Run*)

- **3D technology enhancements successfully demonstrated in 3DL1 Run**
  - **Stacked 3D-vias for electrical and thermal interconnect**
  - **2X reduction in 3D-via size**
  - **Improved tier-to-tier overlay**

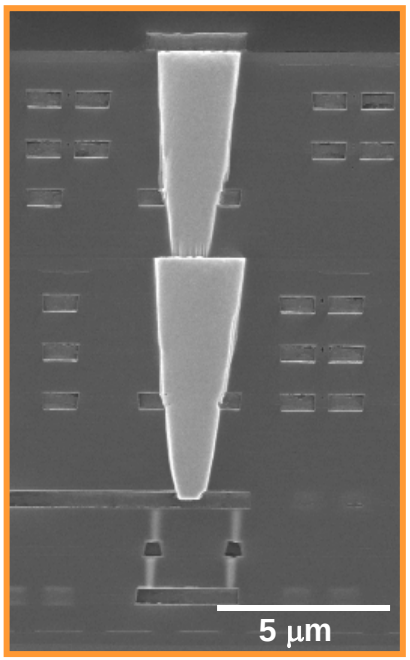
High-Yield on >5000-link Scaled 3D-via Chains



Scaled



Conventional



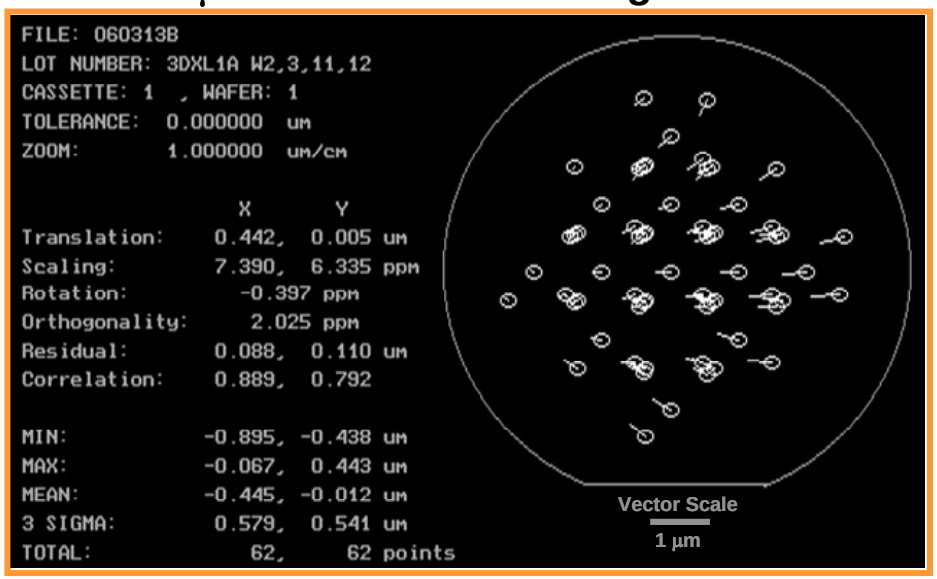
Stack 3D-vias demonstrated

>95% yield on 4800 link chains

Stacked 3D-via resistance ~1Ω

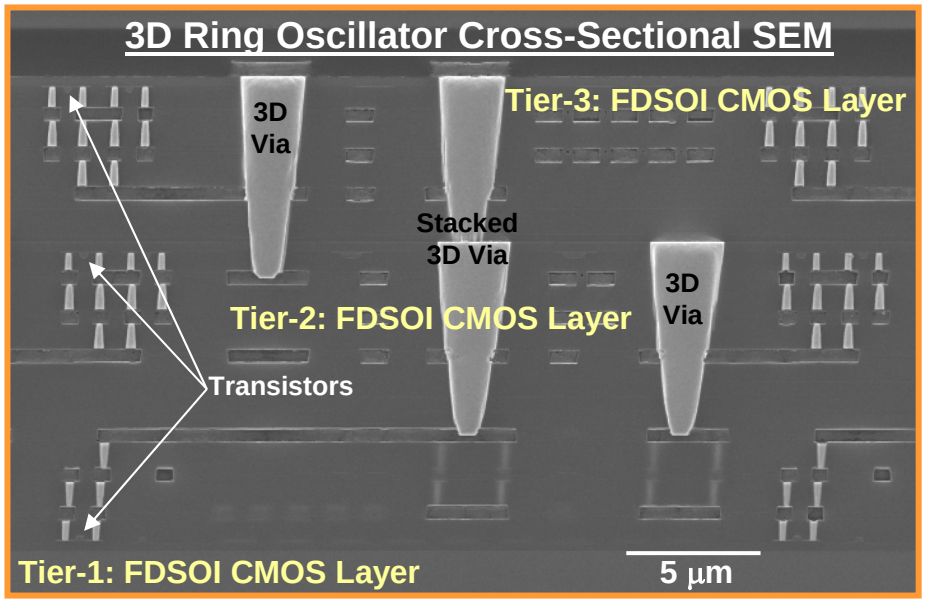
Can be used as thermal vias

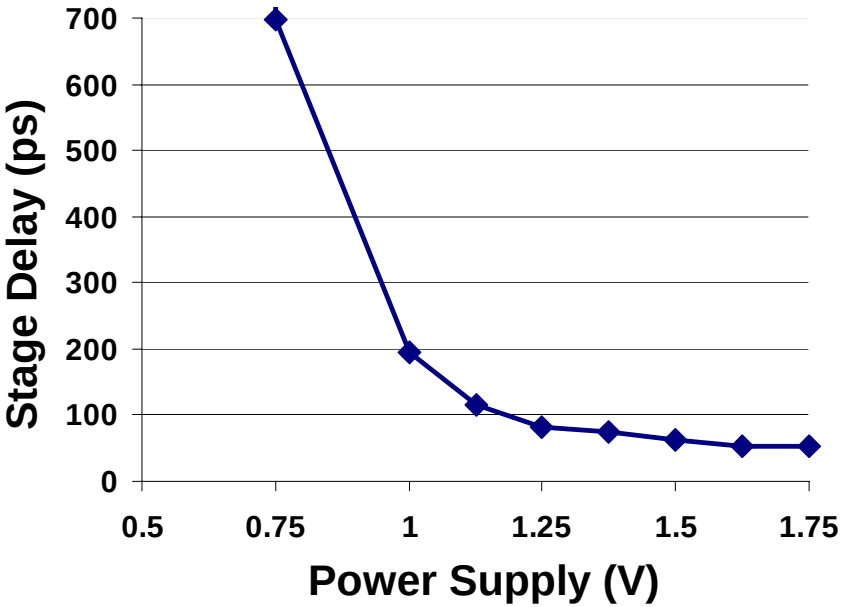
~0.5 μm 3σ Tier-to-Tier Registration

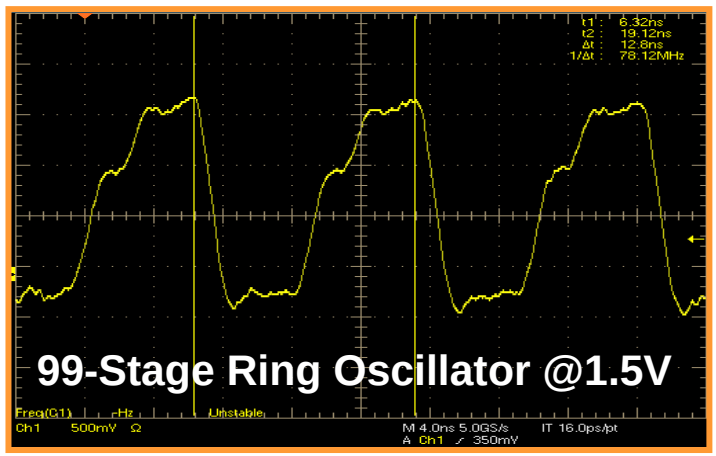


3-Tier, 3D-Integrated Ring Oscillator
(DARPA 3DL1 *Multiproject Run*)

- **Functional 3-tier, 3D-integrated ring oscillator**
  - **Uses all three active transistor layers, 10 levels of metal and experimental *stacked 3D-vias***
  - **Demonstrates viability of 3D integration process**

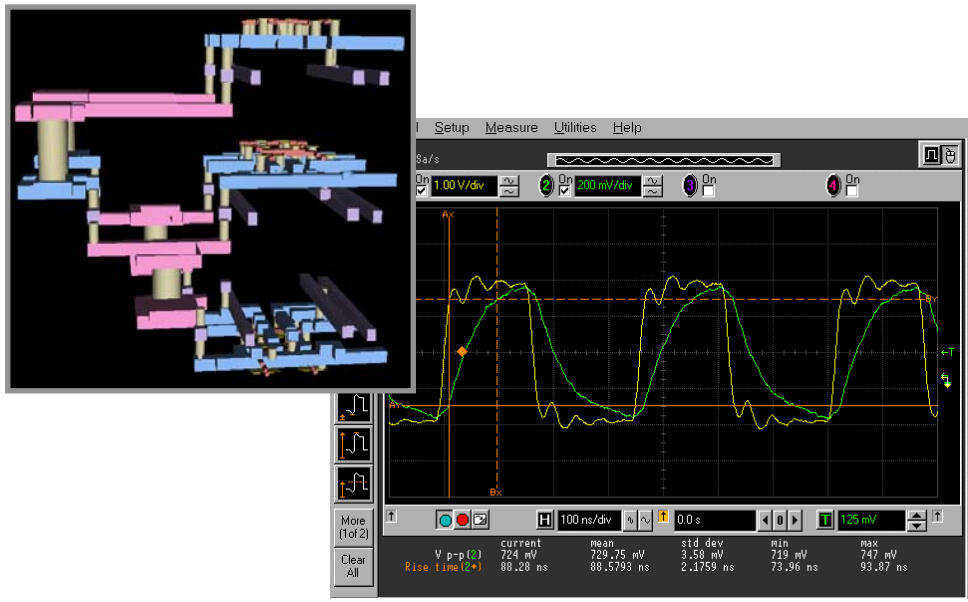




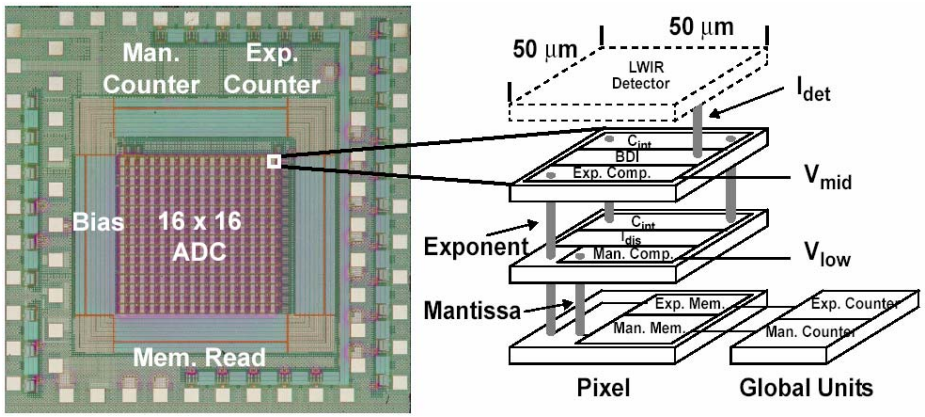


3D IC Multiproject Run Highlights (a)

- **RPI, Jack McDonald (PI)**
  - ✓ ***Designed high-bandwidth 3D SRAM for high-performance computing applications***
  - ✓ ***Demonstrated first functional 3D-integrated, 3-tier memory***



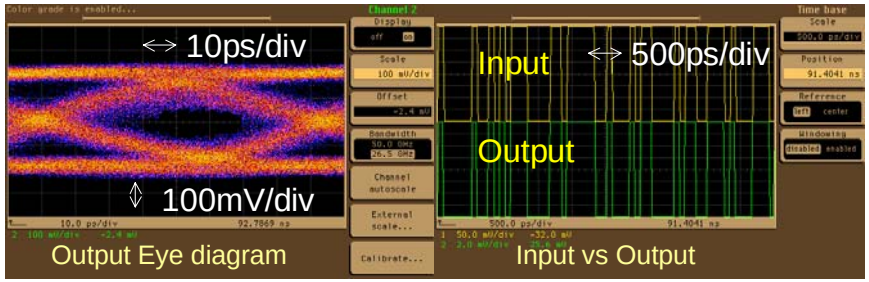
- **Stanford Univ., Sang-Min Lee, Bruce Wooley (PI)**
  - ✓ ***Designed and demonstrated high dynamic range (18-19 bit) high frame rate (3000 fps) 3D ADC for LWIR focal plane array readouts***
  - ✓ ***Reduced pixel size for complex readout to 50 μm x 50 μm***



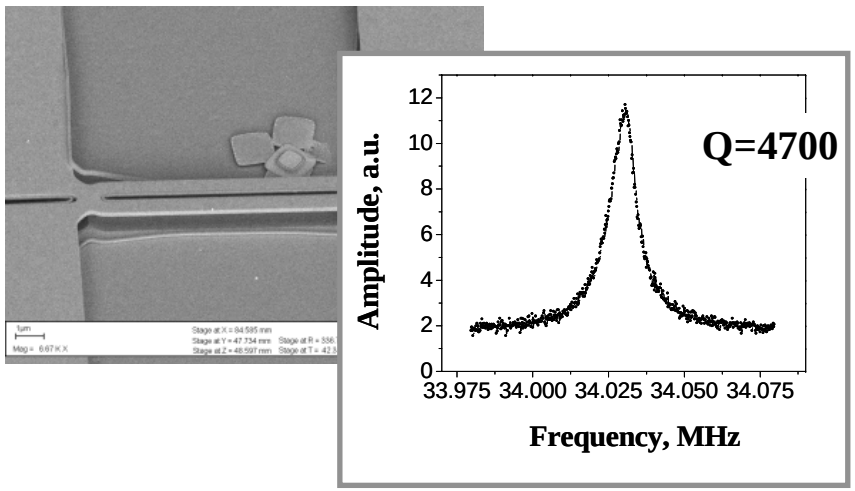
3D IC Multiproject Run Highlights (b)

- **UCLA, Frank Chang (PI)**
  - ✓ ***Designed low power, low BER 10Gbps capacitor-coupled vertical Interconnects for 3D-IC***
  - ✓ ***Demonstrated Baseband Impulse Shaping Interconnect (BISI) and self-synchronized RF Interconnect (RFI) at >11 GHz with BER < $1x10^{-14}$***
  - ✓ ***>10x lower energy/bit and >3x faster than previously reported 180-nm 2D communication circuits***
- **NRL-Cornell-BAE, Maxim Zalalutdinov (PI)**
  - ✓ ***Designed 3D CMOS-integrated high frequency, high quality factor micromechanical resonators***
  - ✓ ***Demonstrated tuning fork and slot resonators at 34MHz with Q = 4700***

RFI Test @ 12.5 GHz data rate

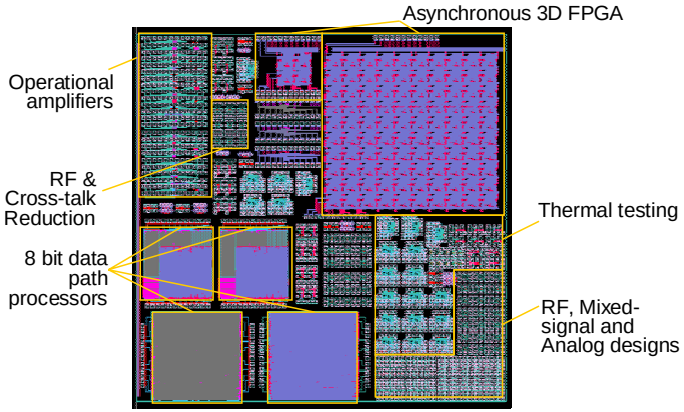


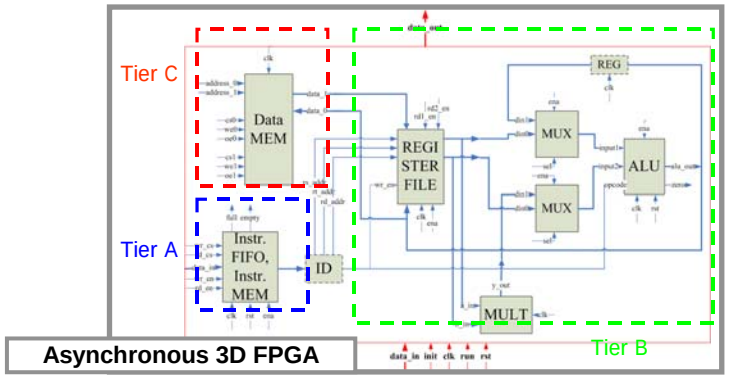
Post Process Released Resonator



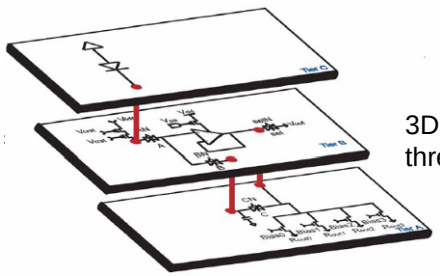
3D IC Multiproject Run Highlights (c)

- **Cornell Univ., Sandip Tiwari (PI)**
  - ✓ ***Designed full range of 3D test structures and circuits***
  - ✓ ***Characterized 3D heat dissipation***
  - ✓ ***Demonstrated functional asynchronous 3D FPGA***
  - ✓ ***Demonstrated low voltage adaptive analog circuits with backgating***
  - ✓ ***Demonstrated RF cross-talk reduction through 3D-integrated ground planes***





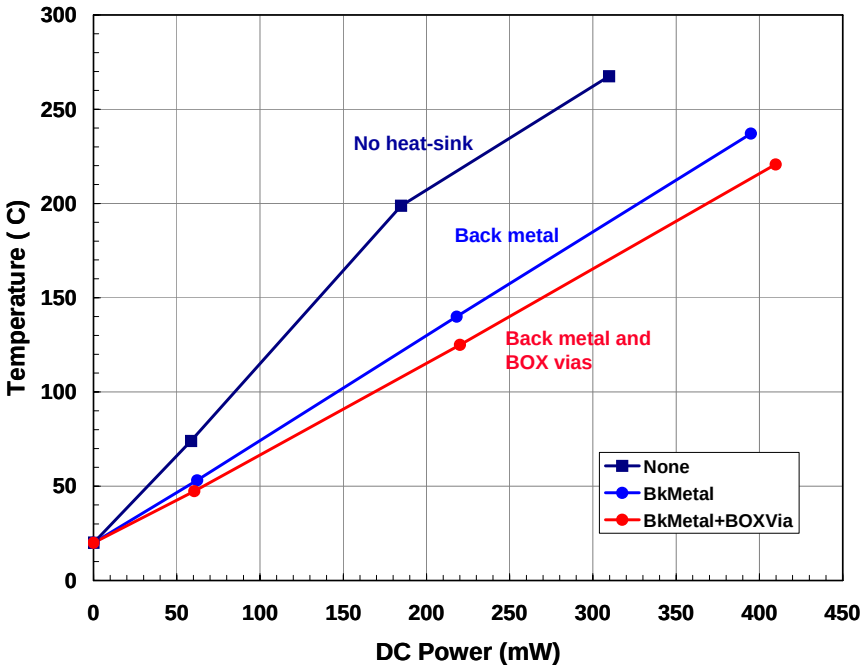
- **Yale Univ., Eugenio Culurciello (PI)**
  - ✓ ***Designed 3D integrated detector sensitive to intensity, contours, and motion***
  - ✓ ***Demonstrated functionality of single and multiple tier photo detectors***



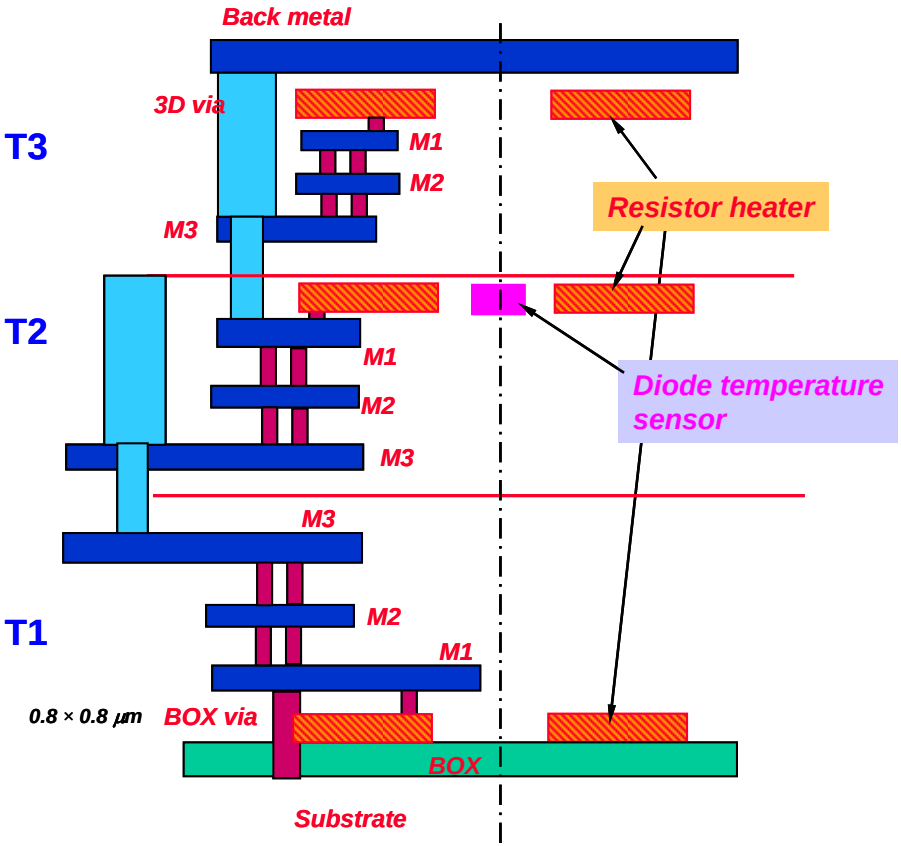
3D pixel view
three 3D vias per pixel

Temperature Measurement Results from 3DL1 Multiproject Run

- **Thermal characterization structures included in 3DL1 Multiproject Run**
  - **Measure temperatures in stack**
  - **Explore thermal sink paths through buried oxide (BOX) vias and "Back-metal" hear sinks**
  - **Calibrate thermal modeling tools**



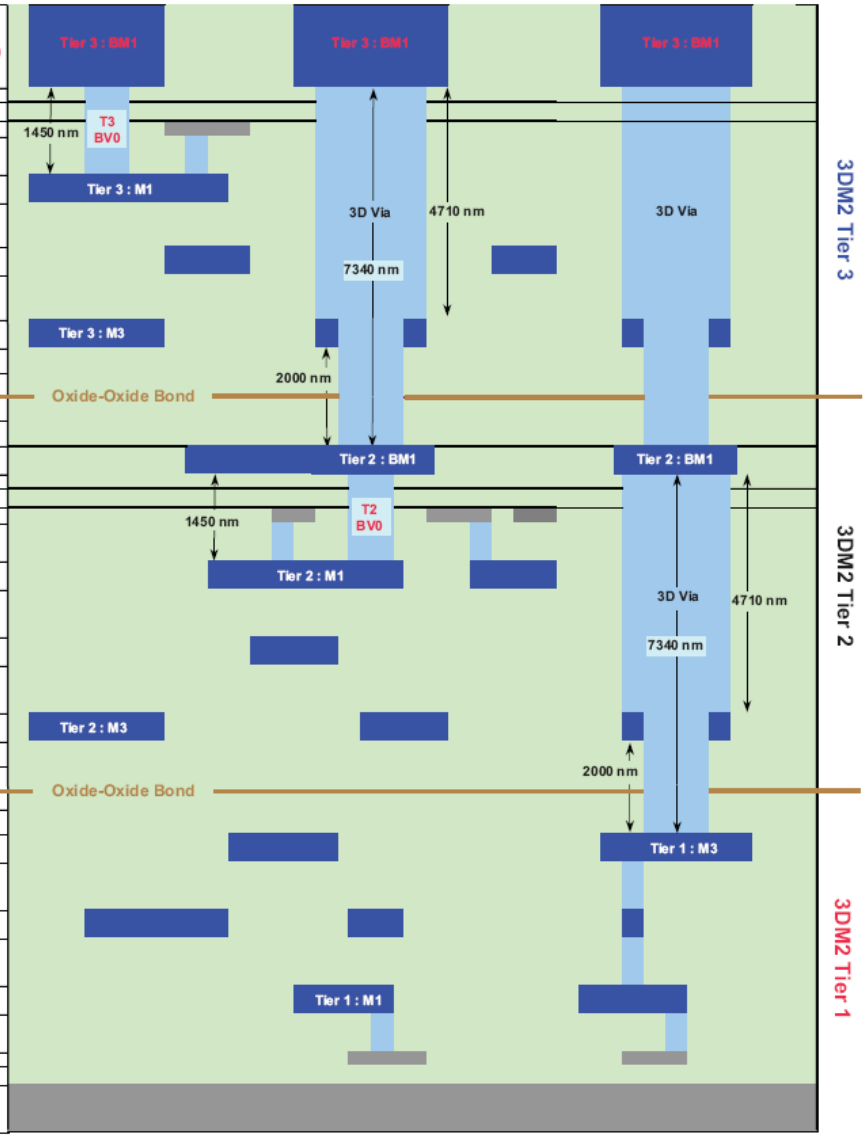
3D Temperature Characterization Structure



3DM2 Multiproject Run
(3 Active Tiers, 11 levels of Metal)

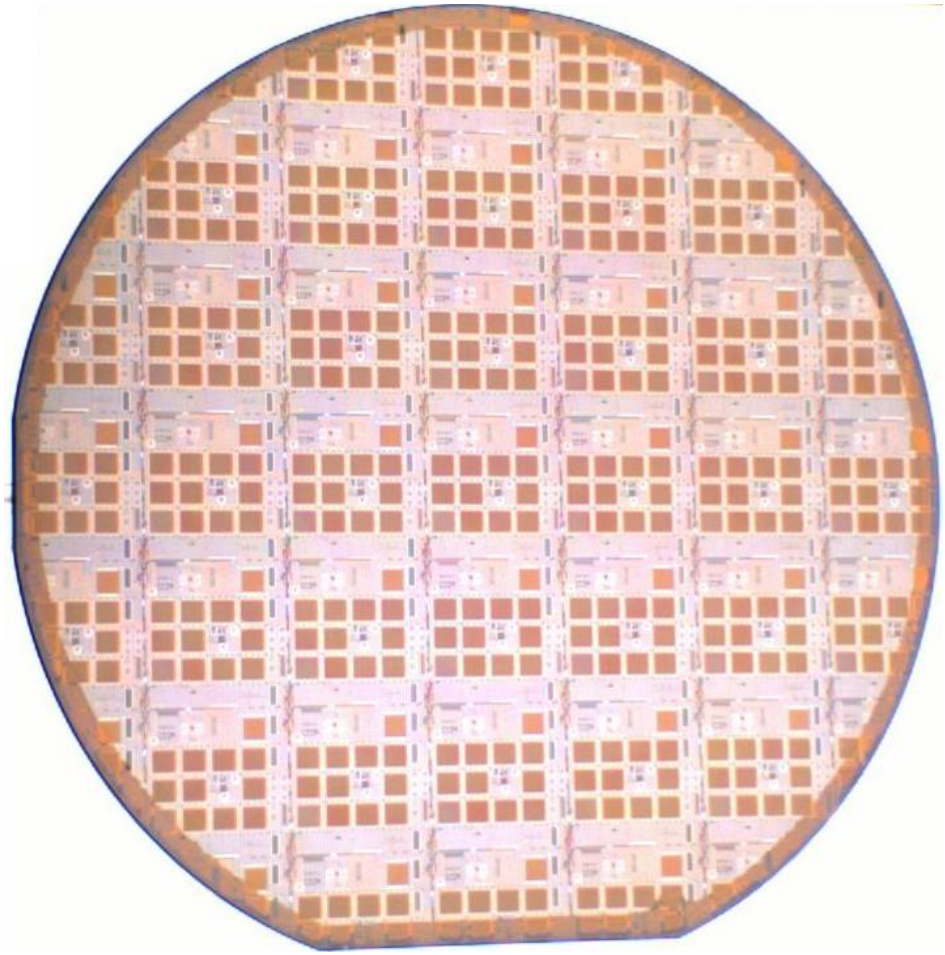
- 3DM2 includes 2 “digital” 180-nm FDSOI CMOS tiers and 1 RF 180-nm FDSOI CMOS tier
  - 11 metal layers including:
    - 2-μm-thick RF Backmetal
    - Tier-2 Backmetal
- Second 3D Multiproject Design Schedule (3DM2)
  - 3DM2 announcement (Mar 06)
  - Contributor selection (Apr 06)
  - Design guide release (Apr 06)
  - Submission deadline (November 06)

Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	



3D-Integration with III-V Detectors

- Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors
  - Tight pixel-pitch IR focal planes and APD arrays
  - InGaAsP (1.06-μm), InGaAs (1.55-μm)
- High-yield, 3.4 μm pitch 3D-via chains demonstrated



150-mm-diameter InP wafer with oxide-bonded circuit layer transferred from silicon wafer

Summary
A Few Closing Remarks…

- Transistor feasibility has been demonstrated to below ~10 nm gate lengths
- "Conventional" CMOS (Bulk, SiO_2 gate oxide, poly gates) faces significant challenges to scale below 45nm-node
  - Ultra-thin-body SOI, FinFET, Dual-Gate, Metal Gate, High-k
  - No new device technology has yet emerged that is expected to dethrone silicon CMOS
- Moore's Law scaling is showing its age and could run into serious speedbumps in the next few years (including economics), but the 2020 roadmap is theoretically feasible
  - Process technology improvements are no longer the performance drivers
- Future performance improvements will most likely come through circuit, system architecture, and software advancements
- Initial 3D technology demonstrations (at MIT-LL) are centered around advanced focal plane architectures
  - This is the "low hanging fruit"
- Full impact of 3D integration is far from being realized, but has the potential of revolutionizing the design architecture of future circuits and systems
- Potential application areas include: High-end focal planes, FPGAs, Dense memory, memory on processor, mixed signal systems, mixed material systems